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A New Interleaved Three-Phase Single-Stage PFC AC-DC Converter with Flying Capacitor

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***Abstract*— A new interleaved three-phase PFC AC-DC single-stage multilevel is proposed in this paper. The proposed converter can operate with reduced input current ripple and peak switch currents due to its interleaved structure, a continuous output inductor current due to its three-level structure, and improved light-load efficiency as some of its switches can be turned on softly. In the paper, the operation of the converter is explained, the steady-state characteristics of the new converter are determined and its design is discussed. The feasibility of the new converter is confirmed with experimental results obtained from a prototype converter and its efficiency is compared to that of another multilevel converter of similar type.**

***Index Terms*— AC-DC power factor correction, Single-stage converters, Three-Phase Systems, Three level converters, Phase-shifted modulation.**

I. Introduction

AC-DC power supplies need to be implemented with some sort of input power factor correction (PFC) to comply with harmonic standards such as IEC 1000-3-2 [1]. PFC techniques can generally be classified as follows:

- Passive methods that use inductors and capacitors to filter out low frequency input current harmonics to make the input current more sinusoidal. Although these converters implemented with such PFC are simple and inexpensive, they are also heavy and bulky and thus passive methods are used in a limited number of applications.

- Two-stage converters that use a pre-regulator to make the input current sinusoidal and to control the intermediate DC bus voltage along with a DC-DC converter to produce the desired output voltage. Such converters, however, require two separate switch-mode converters so that the cost, size, and complexity of the overall ac-dc converter is increased.

- Single-stage power-factor-corrected (SSPFC) converters that have PFC and isolated DC-DC conversion in a single power converter so that they are simpler and cheaper than two-stage converters. Several single-phase [2]-[4] and three-phase [5]-[16] converters have been proposed in the literature, with three-phase converters being preferred over single-phase converters for higher power applications.

Previously proposed three-phase single-stage AC-DC converters, however, have at least one of the following drawbacks that have limited their widespread use:

- They are implemented with three separate AC-DC single-stage modules [5]-[7], which increases cost and introduces issues related to the synchronization of all three modules.
- The converter must be implemented with switches and bulk capacitors with very high voltage ratings as they are exposed to very high voltages [9], [10], [13], [14].
- The converter has difficulty performing PFC and DC-DC conversion simultaneously, which results in significant input current distortion [8].
- The converter must be controlled using very sophisticated techniques and/or non-standard techniques [2]-[4]. This is especially true of resonant type converters that need variable switching frequency control methods to operate.
- The converter has a very high output ripple as its output current must be discontinuous. Secondary diodes with high peak current ratings and large output capacitors to filter the ripple are needed [5]-[11].
- There is a need to have a large input filter to filter out large input current ripple as this current is discontinuous with high peaks [5]-[6], [9], [10],[13]-[16].

A three-phase, single-stage three-level converter proposed in [16] mitigates these drawbacks. Although the converter proposed in that paper was an advance over previously proposed three-phase single-stage converters, it still suffered from the need to have a discontinuous output inductor current at light load conditions to keep the DC bus capacitor voltage less than 450V and it needed to operate with discontinuous input current, which resulted in high component current stress and the need for significant input filtering due to the large amount of ripple.

The topology proposed in [17], which is shown in Fig. 1, is an interleaved three-phase, single-stage converter that has an interleaved structure, which this structure is a very popular structure in power electrons converters [18]-[21]. The topology in [17] also has an output current that is continuous for almost all load ranges, a DC bus voltage that is less than 450 for all load conditions and a superior input current harmonic content.

In this paper, a new interleaved three-phase single-stage PFC AC-DC converter that uses flying capacitor structure with standard phase-shift PWM, are shown in Fig. 2 and 3, is

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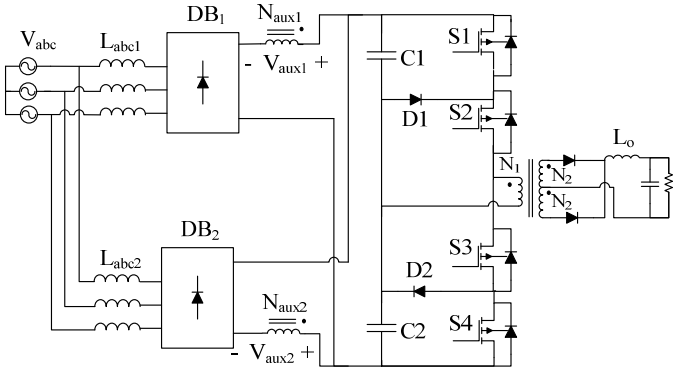

Fig. 1. An interleaved three-phase three-level converter [17].

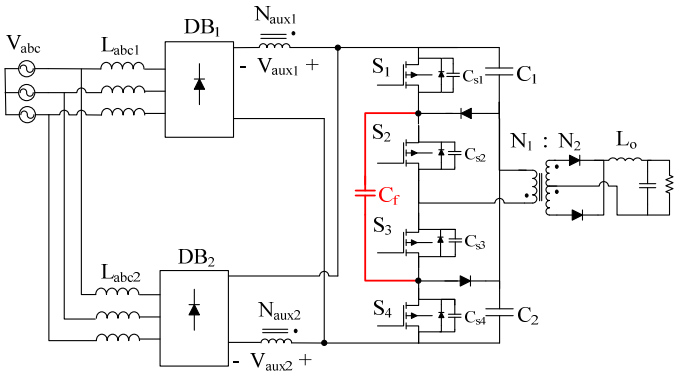

Fig. 2. Proposed single-stage three-level ac-dc converter.

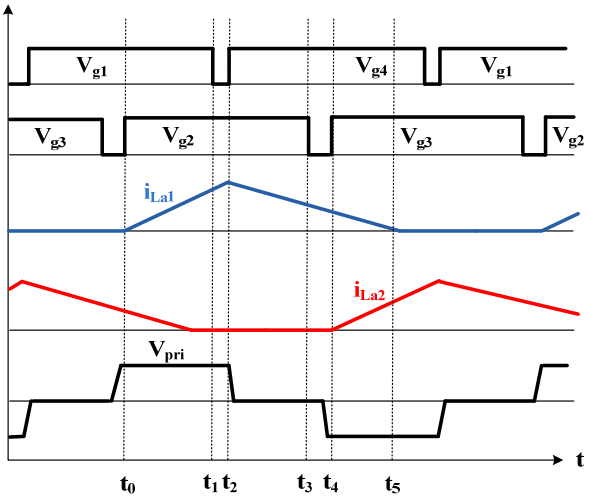

Fig. 3. Typical waveforms for proposed converter

presented to improve efficiency of the converter particularly at light load conditions. The operation of the converter is explained, the steady-state characteristics of the new converter are determined and its design is discussed. The feasibility of the new converter is confirmed with experimental results obtained from a prototype converter and its efficiency is compared to that of another multilevel converter of similar type.

II. Converter Topology

The converter and its key waveforms are shown in Figs. 2 and 3. The proposed converter uses auxiliary windings that are taken from the converter transformer to act as "magnetic switches" to cancel the DC bus capacitor voltage so that the voltage that appears across the diode bridge output is zero. Auxiliary Winding 1 (N_{aux1}/N_1=2) cancels out the DC bus voltage when the primary voltage of the main transformer is positive, so that the output voltage of Diode Bridge 1 (DB_1) is zero and the currents in input inductors L_{a1}, L_{b1}, and L_{c1} rise. Auxiliary Winding 2 (N_{aux2}/N_1=2) cancels out the DC bus voltage when the primary voltage of the main transformer is negative, so that the output voltage of Diode Bridge 2 (DB_2) is zero and the currents in input inductors L_{a2}, L_{b2}, and L_{c2} rise.

When there is no voltage across the main transformer primary winding, the total voltage across the DC bus capacitors appears at the output of the diode bridges and the input currents falls since this voltage is greater than the input voltage. If the input currents are discontinuous, the envelope of the input current will be sinusoidal and in phase with the input voltages.

The converter has the following modes of operation during a half switching cycle; equivalent circuit diagrams that show the converter's modes of operation are shown in Fig. 4:

Mode 1 ($t_0 < t < t_1$): During this interval, switches S_1 and S_2 are ON. It should be noted that both DC bus capacitors and the flying capacitor are charged to half of the DC bus voltage. In this mode, energy from DC bus capacitor C_1 flows to the output load. Due to magnetic coupling, a voltage appears across Auxiliary Winding 1 that is equal to the DC bus voltage, but with opposite polarity. This voltage cancels the total DC bus capacitor voltage so that the voltage at the diode bridge output is zero and the input currents in L_{a1}, L_{b1}, and L_{c1} rise.

Mode 2 ($t_1 < t < t_2$): In this mode, S_1 is OFF and S_2 remains ON. Capacitor C_{s1} charges and capacitor C_{s4} discharges through C_f until the voltage across C_{s4}, the output capacitance of S_4, is clamped to zero. The energy stored in the input inductor during the previous mode starts being transferred into the DC bus capacitors. This mode ends when S_4 turns on with ZVS.

Mode 3 ($t_2 < t < t_3$): In Mode 3, S_1 is OFF and S_2 remains ON. The energy stored in input inductor L_1 during Mode 1 is transferring into the DC bus capacitors. The voltage that appears across Auxiliary Winding 1 is zero. The primary current of the main transformer circulates through D_1 and S_2. With respect to the converter's output section, the load inductor current freewheels in the secondary of the transformer, which defines a voltage across the load filter inductor that is equal to $-V_L$.

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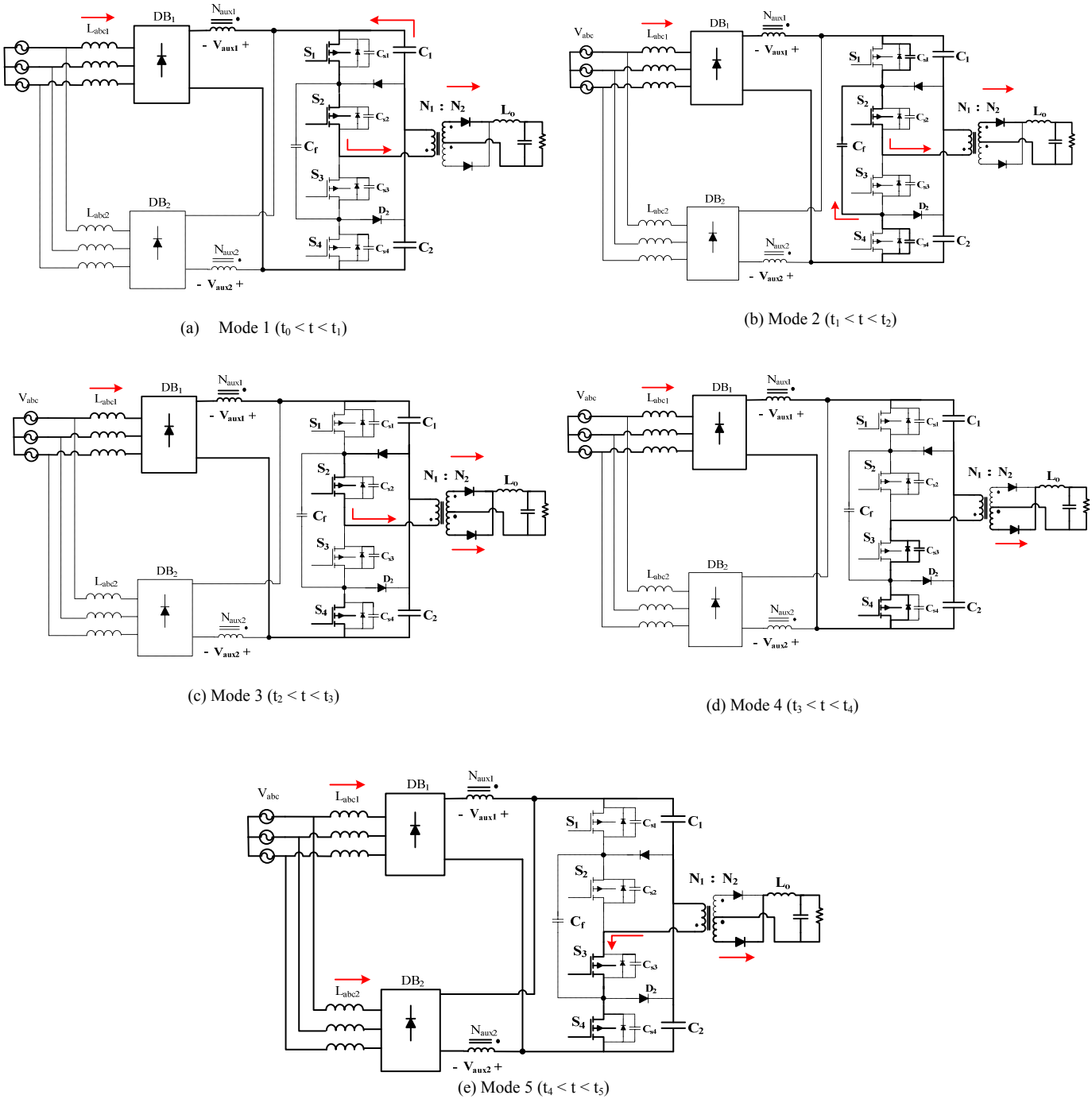

(a) Mode 1 ($t_0 < t < t_1$)

(b) Mode 2 ($t_1 < t < t_2$)

(c) Mode 3 ($t_2 < t < t_3$)

(d) Mode 4 ($t_3 < t < t_4$)

(e) Mode 5 ($t_4 < t < t_5$)

Fig. 4. Modes of operation.

Mode 4 ($t_3 < t < t_4$): In this mode, S_1 and S_2 are OFF. The energy stored in L_1 continues to be transferred into the DC bus capacitor. The primary current of the transformer discharges the output capacitor of C_{s3}. If there is enough energy in the leakage inductance, the primary current will completely discharge the body capacitor of C_{s3} and current will flow through the body diode of S_3.This current also charges C_2 through the body diodes of S_3 and S_4. Switch S_3 is switched ON at the end of this mode.

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Mode 5 ($t_4 < t < t_5$): In this mode, S_3 and S_4 are ON and energy flows from capacitor C_2 to the load. A voltage appears across Auxiliary Winding 2 that is equal to the DC bus voltage, but with opposite polarity to cancel out the DC bus voltage. The voltage across the boost inductors L_2 (L_2= L_{abc2}) becomes only the rectified supply voltage of each phase and the current flowing through each inductor increases. This mode ends when the energy stored in L_1 is completely transferred into the DC bus capacitor. For the remainder of the switching cycle, the converter goes through Modes 6 to 10, which are identical to Modes 1 to 5 except that S_3 and S_4 are ON instead of S_1 and S_2 and DB_2 conducts current instead of DB_1.

The input current is the sum of currents i_{L1} and i_{L2}, corresponding to each set of input inductors, with each inductor having a discontinuous current. However, by selecting appropriate values for $L_{a1} = L_{b1} = L_{c1}$ and $L_{a2} = L_{b2} = L_{c2}$, two inductor currents such as i_{La1} and i_{La2} can be made to overlap each other so that the input current can be made continuous; thus reducing the size of input filter significantly. There is a natural 180° phase difference between the currents in L_1 and the currents in L_2 as one set of currents rises when the transformer primary is impressed with a positive voltage and the other set rises when the transformer primary is impressed with a negative voltage.

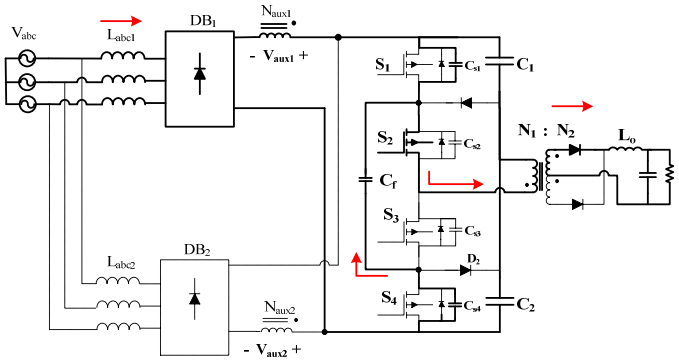
It should be noted that standard phase-shift PWM can be implemented in the converter and thus a standard phase-shift PWM IC can be used to generate the gating signal. This can be seen from Fig. 3 and the modal circuit diagrams. Switches S_2 and S_3 are not allowed to be ON at the same time and switches S_1 and S_4 are not allowed to be ON simultaneously as well. The converter is in an energy-transfer mode whenever switches S_1 and S_2 are ON or S_3 and S_4 are ON. It is in a freewheeling mode of operation whenever switches S_1 and S_3 or S_2 and S_4 are ON. The sequence of alternating energy-transfer and freewheeling modes that occur during a switching cycle corresponds to the same sequence of modes that exists in a standard two-level phase-shift PWM full-bridge converter.

III. Flying Capacitor vs. Diode-Clamped Multilevel Three-Phase Single-Stage Converter

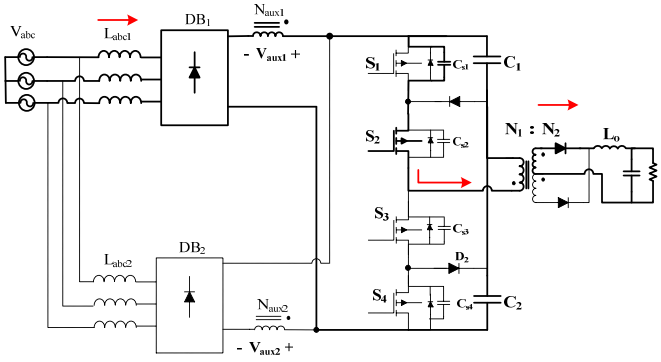
The proposed interleaved topology with flying capacitor can guarantee a ZVS turn-on for its very top and very bottom switches in a way that the converter presented in [17] cannot. To understand why this is so, first consider a standard two-level ZVS-PWM DC-DC full-bridge converter operating with phase-shift PWM. For this converter, the leading leg switches (switches that are turned ON when the converter enters a freewheeling mode of operation) of this converter can be turned on with ZVS. This is due to the fact that the transformer primary current is dominated by reflected output inductor current during this transition so that there is sufficient energy available to turn ON the leading leg switches with ZVS. It is the lagging leg switches (switches that are turned ON when the converter is exiting a freewheeling mode) that lose their ability to turn ON with ZVS under light-load conditions as it is only the transformer primary leakage inductance energy that is available to discharge and charge the appropriate switch output capacitances.

Now consider the converter proposed in [17], as shown in Fig. 5(b). It can be seen in Fig. 5(a) that the converter enters a freewheeling mode of operation when switch S_1 is turned OFF. The converter exits this freewheeling mode by the turning OFF of S_1 and then the simultaneous turning ON of switches S_3 and S_4. During this transition, it is only the leakage inductance energy that is available to turn S_3 and S_4 ON with ZVS. Similarly, switch S_1 and S_2 are turned ON when the converter exits the other freewheeling mode of the switching cycle, again, with only the leakage inductance energy available to discharge their output capacitances. What this means is that all the converter switches lose the ability to turn ON with ZVS under light-load conditions as only leakage inductance energy is available to discharge their output capacitances just before they are turned ON.

With respect to the proposed converter, as can be seen from Mode 2 (just like Mode 7), shown in Fig. 5(a), when S_1 (or S_4) turns off and the converter enters a freewheeling mode of operation, the energy available to charge the output capacitance of S_1 (or S_4 in Mode 7) and discharge the output capacitance of S_4 (or S_1 in Mode 7) is the energy stored in leakage inductance plus the energy in output filter inductor



(a) Mode 2 in proposed flying capacitor converter ($t_1 < t < t_2$)



(b) Mode 2 in diode-clamped converter [17] (t0 < t < t1)

Fig. 5. Flying capacitor vs. diode-clamped three-phase single-stage converter

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that is "reflected" to the primary. Since the energy in the filter inductor is large compared to that required to charge/discharge the capacitances, the body capacitance of S_4 (or S_1 in Mode 7) can be discharged completely through flying capacitor C_f. Once this happens, switch S_4 (or S_1 after Mode 7) can be turned ON with ZVS in anticipation for later on in the switching cycle when the converter exits a freewheeling mode of operation.

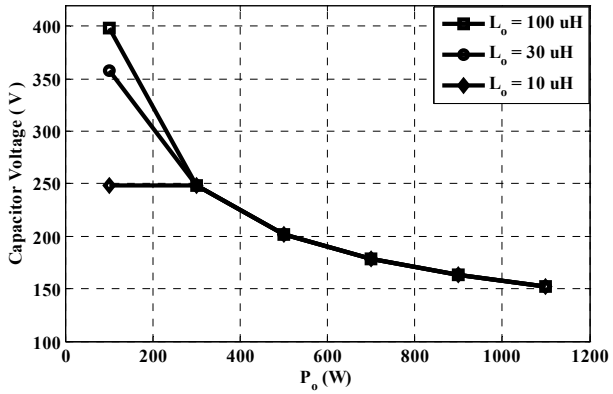
The ZVS turn-on for switches S_1 and S_4, when the converter is exiting a freewheeling mode of operation cannot happen for the converter presented in [17], as can be seen in Fig. 5(b). This is because there is no flying capacitor in the converter that provides a path for current to flow through when the converter enters a freewheeling mode of operation. These switches can only turn ON with ZVS if there is sufficient transformer leakage inductance energy to discharge the output capacitance of these devices when the converter is exiting a freewheeling mode of operation. Since this is rarely the case when the converter is operating under light load conditions, these switches will not turn ON with ZVS. As a result, the proposed converter with flying capacitor has a better light-load efficiency than the converter proposed in [17] because two of its switches can always turn ON with ZVS, regardless of the load.

IV. Converter Analysis

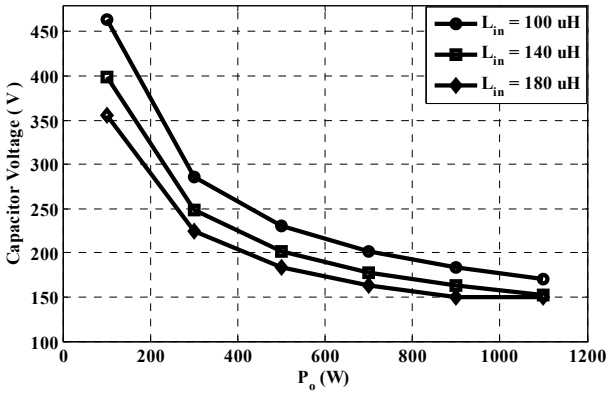
The analysis and design of the proposed converter is almost identical to that presented in [16]-[17] and is therefore are not presented here, in detail. Only graphs of key characteristic curves and general design guidelines are presented in this paper. The reader is referred to [16]-[17] for details.

In order to analyze and determine the steady-state operating points of the converter, a computer program such as the one presented in [16] has been used. Graphs of steady-state characteristics, such as the ones shown in Fig. 6, can be used as part of a design procedure. These graphs help to find out the appropriate parameter values based on the defined operating point.

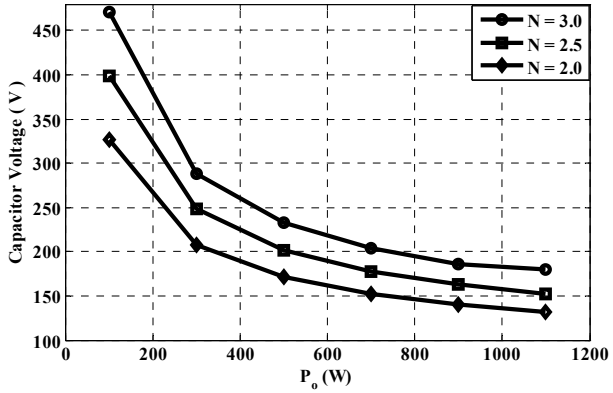
Assuming ideal operation to simplify the analysis, the characteristic curves of the proposed converter and the converter proposed in [17] are the same. This is because in this case, the flying capacitor just affects the transition modes of the converter and does not affect the overall steady state operation of the proposed converter.



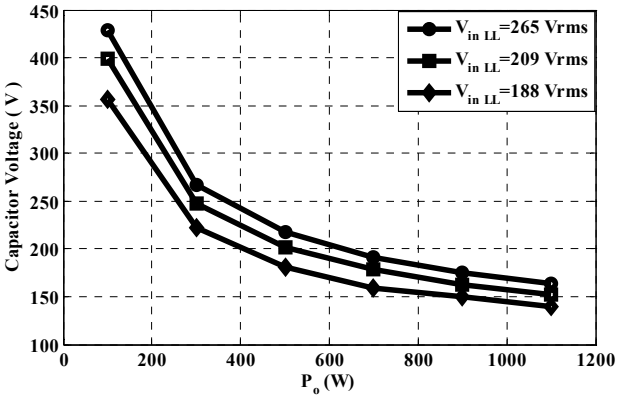
(a) Effect of output inductor value L_o on dc bus voltage



(b) Effect of input Inductor value L_{in} on dc Bus Voltage



(c) Effect of transformer ratio value N on dc bus voltage



(d) Effect of input voltage v_{in} on dc bus voltage

Fig.6. Steady-State characteristic curves (V_{in}=208V_{rms}, Vo=48V, f_{sw}=100kHz).

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V. Design Guidelines

General considerations that should be taken into account when trying to design the proposed converter are discussed in this section of the paper. The key parameters values in the design of the converter are output inductor L_o, transformer turns ratio N and input inductor L_{in}. The following should be considered when trying to select values for these components:

A. Transformer turns ratio N:

The value of N affects the primary-side dc bus voltage. It determines how much reflected load current is available at the transformer primary to discharge the bus capacitors. If N is low, the primary current may be too high and thus the converter will have more conduction losses. If N is very high, then the amount of current circulating in the primary-side is reduced, but the primary current that is available to discharge the dc-link capacitors may be low and thus dc bus voltage may become excessive under certain operating conditions (i.e. high line). The minimum value of N can be found by considering the case when the converter must operate with minimum input line and, thus, minimum primary-side dc bus voltage and maximum duty cycle. If the converter can produce the required output voltage and can operate with discontinuous input and continuous output currents in this case, then it can do so for all cases.

B. Output inductor L_o:

The output inductor should be designed so that the output current is made to be continuous under most operating conditions, if possible. The minimum value of L_o should be the value of L_o with which the converter's output current will be continuous on the when the converter is operating with maximum input voltage, minimum duty cycle and minimum load. If this condition is met, then the output current will be continuous for all other converter's operating conditions. On the other hand, the value of L_o cannot be too high as the dc bus voltage of the converter may become excessive under very light loads conditions.

C. Input inductor L_{in}:

The value for L_1 and L_2 should be low enough to ensure that their currents are fully discontinuous under all operating conditions, but not so low as to result in excessively high peak currents. It should be noted that input current is summation of inductor currents i_{L1} and i_{L2} which are both discontinuous. However, by selecting appropriate values for L_1 (= L_{a1} = L_{b1} = L_{c1}) and L_2 (= L_{a2} = L_{b2} = L_{c2}) in such a way that two inductor currents such as i_{La1} and i_{La2} have to overlap each other, the input current can be made.

D. Flying Capacitor C_f:

The flying capacitor is charged to half of the dc bus voltage. When the converter is operated with phase-shift PWM control, as shown in Fig. 3, C_f is generally decoupled from the converter except during certain switching transitions, such as when S_1 is turned off to start Mode 2 and when S_4 is turned off during the equivalent mode later in the switching cycle; therefore there is little opportunity for C_f to charge and discharge during a switching cycle. As a result, the converter can be designed according to the design procedure given in [17] as the operation of the two converters is very similar.

The following expression states the relation between C_f and its ripple voltage based on reflected load current:

$$C_f = \frac{I \,.\, \Delta t}{\Delta V_{Cf}} = \frac{I_o\,(0.5 - D_{max})}{N\, f_s\ \ \Delta V_{Cf}} \qquad (1)$$

where I_o is output current, D_{max} is maximum duty cycle, N is transformer turns ratio, f_s is switching frequency and ΔV_{Cf} is the peak-to-peak ripple voltage of C_f. For maximum load P_o = 1.1kW and output voltage V_o = 48 V, the output current is I_o = 23 A. If the maximum duty cycle is assumed to be D_{max} = 0.4, the transformer turns ratio is N=2.5 and the switching frequency is f_{sw} = 100 kHz, then a 0.5% ripple for flying capacitor voltage results in $\Delta V_{Cf} = 0.005 * 400 = 2\text{V}$ so that the minimum value for C_f according to equation (1) is $C_f = 4.6\ \mu F$.

VI. Experimental Results

An experimental prototype of the proposed three-level converter and the converter shown in Fig. 1 were built to compare their performance. The prototypes were designed according to the following specifications:

Input voltage	V_{in} = 208±10% Vrms (line-line),
Output voltage	V_o = 48 V,
Output power	P_o = 1.1kW,
Switching frequency	f_{sw} = 100 kHz.

The proposed converter was implemented with phase-shift modulation using a UC 2879 phase-shift PWM IC. It should also be noted that no attempt was made to optimize the prototype magnetics and layout and the prototypes that were built were merely proof-of-concept prototypes aimed to confirm certain concepts. The main switches were IRFP27N60KPbF, and the diodes were UF1006DICT. The components were L_{in} = 140 µH, L_o = 100 µH and C_1, C_2, C_f = 2200 µF. The auxiliary transformer ratio was 1:2 and the main transformer ratio was 2.5:1.

Typical waveforms are shown in Fig. 7. Fig. 7(a) shows input voltage and current, and Fig. 7(b) shows the voltage across the primary side of the main transformer of the new converter. Fig.7(c) shows the voltage and current of the switch S_4.

It can be seen that the proposed converter can operate with nearly sinusoidal input currents with no deadband regions. It is a multilevel full-bridge converter that the switch stresses is half the dc bus voltage; it also can operate with a continuous output current, unlike most other converters of the same type.

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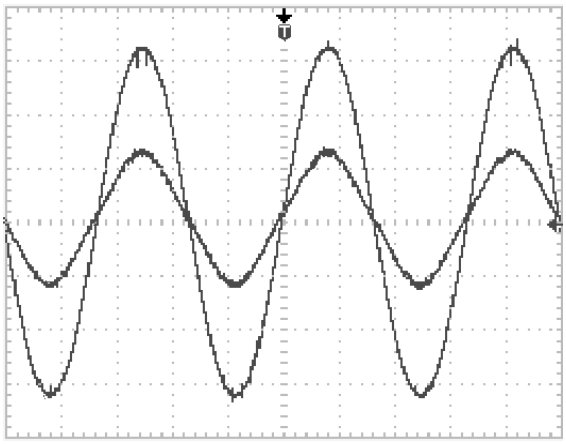
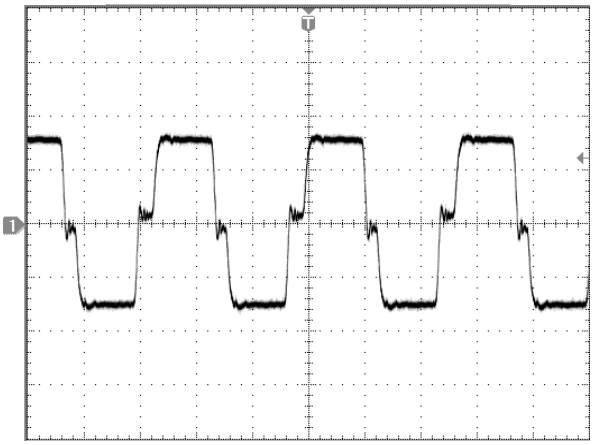
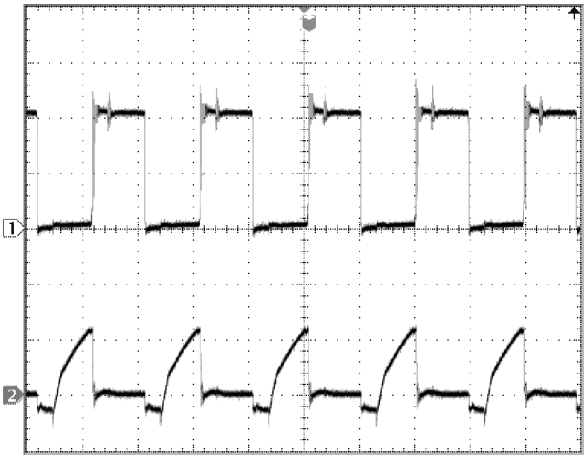


(a) Input current and voltage (V: 100 V/div, I: 4 A/div)



(b) Primary voltage of the main transformer (V:100V/div.,t: 4 μs/div.)



(c) V_{ds} and I_d current of S_4 (V: 100V/div., I:5A/div, t:10 μs/div.s)

Fig. 7. Typical converter waveforms.

Fig. 8 shows a graph of curves of efficiency vs. output load for the two converters. What is of interest in this figure are the characteristics of the two efficiency curves rather than the actual efficiency numbers, which were obtained from proof-of-concept prototypes. It can be seen that that the proposed converter has a higher efficiency that the converter shown in Fig. 1 under light load conditions and that the efficiency of the two converters are almost the same under heavy-load conditions. This is because under light-load conditions, where there is generally insufficient energy to discharge the switch output capacitances when a converter is exiting a freewheeling mode of operation, the new converter has flying capacitor C_f that provides a path to discharge the output capacitance of the very top switch and the very bottom switch before the converter enters a freewheeling mode, as explained in Section III. This is not possible for the converter in proposed in [17]. As a result of the fact that two of its switches can always be turned on with ZVS, the proposed converter has improved efficiency while maintaining all the advantageous features of the converter proposed in [17] such as reduced input current ripple and peak currents, an output current that is continuous over most of the load range, primary switch voltage stresses that are below 450 V_{dc} for all load conditions and a better input current harmonic content then previously proposed converters of the same type. This is not possible for the converter in proposed in [17].

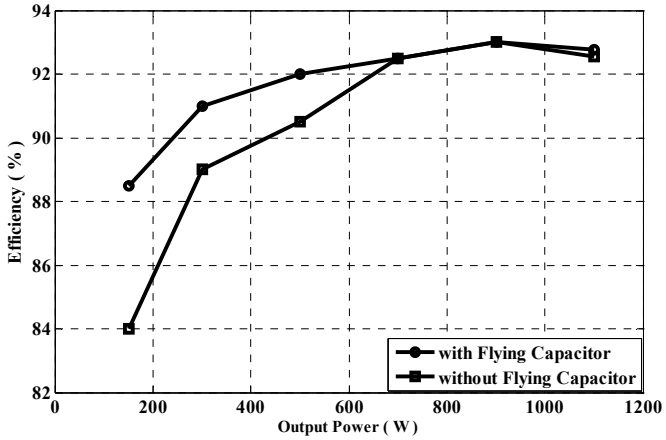


Fig. 8. Efficiency of PWM and PSM three-level single-stage ac-dc converters

VII. Conclusion

A new interleaved three-phase, three-level, single-stage power-factor-corrected AC-DC converter using standard phase-shift PWM was presented in this paper. In this paper, the operation of the converter was explained and its feasibility was confirmed with experimental results obtained from a prototype converter. The efficiency of the new converter was compared to that of another converter of the same type. It was shown that the proposed converter has a better efficiency, especially under light-load conditions, and it was explained that this is because energy from the output inductor can always be used to ensure that the very top and the very bottom switches can be turned ON with ZVS, due to a discharge path that is introduced by its flying capacitor.

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