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A Novel High Step-up DC/DC Converter Based on Integrating Coupled Inductor and Switched-Capacitor techniques for Renewable Energy Applications

Ali Ajami[1], Hossein Ardi[2], and Amir Farakhor[3]
1, 2, 3 Electrical Engineering Department of Azarbaijan Shahid Madani University
email: ajami@azaruniv.edu

***Abstract*—In this paper, a novel high step-up DC/DC converter is presented for Renewable Energy Applications. The suggested structure consists of a coupled inductor and two voltage multiplier cells in order to obtain high step-up voltage gain. In addition, two capacitorsare charged during the switch-off period using the energy stored in the coupled inductor which increases the voltage transfer gain. The energy stored in the leakage inductance is recycled with the use of a passive clamp circuit. The voltage stress on the main power switch is also reduced in the proposed topology. Therefore, a main power switch with low resistance $R_{DS\ (ON)}$can be used to reduce the conduction losses. The operation principle and the steady-state analyses are discussed thoroughly. To verify the performance of the presented converter, a 300W laboratory prototype circuit is implemented. The results validate the theoretical analyses and the practicability of the presented high step-up converter.**

***Index Terms*—Coupled inductor, DC/DC converters, high step-up, switched capacitor.**

I. Introduction

Demand for clean and sustainable energy sources has dramatically increased during the past few years with growing population and industrial development. For a long time, fossil fuels have been used as the major source of generating electrical energy. Environmental consequences of these resources have made it necessary to benefit from clean energy sources such as wind and solar. Therefore, distributed generation (DG) systems based on renewable energy sources have attracted the researchers' attention. The DG systems include photovoltaic (PV) cells, fuel cells and wind power [1]-[3].However, the output voltages of these sources are not large enough for connecting to ac utility voltage. PV cells can be connected in series in order to obtain a large dc voltage. However, it is difficult to ignore the shadow effect in PV panels [4]-[6]. High step-up converters are a suitable solution for the aforementioned problem. Each PV panel can be connected to a particular high step-up converter. Therefore, each panel can be controlled independently. These converters boost the low input voltages (24-40 V) to a high voltage level (300-400 V) [7]. The main features of high step-up converters are their large conversion ratio, high efficiency and small size [8]-[10].

Theoretically, conventional boost converters can achieve high voltage gain with an extremely high duty ratio [11]. However, the performance of the system will be deteriorated with a high duty cycle due to several problems such as low conversion efficiency, reverse-recovery and electromagnetic interference problems [12].

Some transformer-based converters like forward, push-pull or flyback converters can achieve high step-up voltage gain by adjusting the turn ratio of the transformer. However, the leakage inductor of the transformer will cause serious problems such as voltage spike on the main switch and high power dissipation [13]. In order to improve the conversion efficiency and obtain high step-up voltage gain, many converter structures have been presented [14]-[29]. Switched capacitor [14]-[16] and voltage lift [17]-[19] techniques have been used widely to achieve high step-up voltage gain. However, in these structures, high charging currents will flow through the main switch and increase the conduction losses.

Coupled-inductor based converters can also achieve high step-up voltage gain by adjusting the turn ratios [20], [21]. However, the energy stored in the leakage inductor causes a voltage spike on the main switch and deteriorates the conversion efficiency. To overcome this problem, coupled-inductor based converters with an active-clamp circuit have been presented in[22]. Some high step-up converters with two-switch [23]-[25] and single-switch [26]-[29] are introduced in the recent published literatures. However, the conversion ratio is not large enough.

This paper presents a novel high step-up DC/DC converter for renewable energy applications. The suggested structure consists of a coupled inductor and two voltage multiplier cells in order to obtain high step-up voltage gain. In addition, a capacitor is charged during the switch-off period using the energy stored in the coupled inductor which increases the voltage transfer gain. The energy stored in the leakage inductance is recycled with the use of a passive clamp circuit. The voltage stress on the main power switch is also reduced in the proposed topology. Therefore, a main power switch with low resistance $R_{DS\ (ON)}$can be used to reduce the conduction

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losses. The operation principle and the steady-state analyses are discussed thoroughly. To verify the performance of the presented converter, a 300W laboratory prototype circuit is implemented. The results validate the theoretical analyses and the practicability of the presented high step-up converter.

II. Operating Principle of The Proposed Converter

The circuit configuration of the proposed converter is shown in Fig. 1. The proposed converter comprises a DC input voltage (V_I), active power switch (S), coupled inductor, four diodes and four capacitors. Capacitor C_1 and diode D_1 are employed as clamp circuit respectively. The capacitor C_3 is employed as the capacitor of the extended voltage multiplier cell. The capacitor C_2 and diode D_2 are the circuit elements of the voltage multiplier which increase the voltage ofclamping capacitor C_1. The coupled inductor is modeled as an ideal transformer with a turn ratio N (N_P/N_S), a magnetizing inductor L_m and leakage inductor L_k.

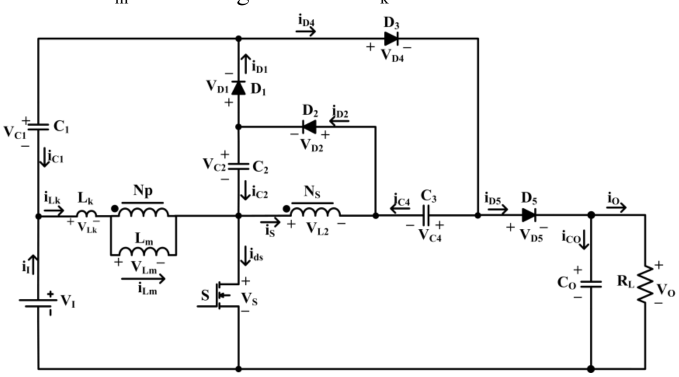


Fig. 1. Circuit configuration of the presented high step-up converter.

In order to simplify the circuit analysis of the converter, some assumptions are considered as follow:

1) All Capacitors are sufficiently large. Therefore V_{C1}, V_{C2}, V_{C3}, and V_O are considered to be constant during one switching period.

2) All components are ideal but the leakage inductance of the coupled inductor is considered.

According to the aforementioned assumptions, the CCM operation of the proposed converter includes five intervals in one switching period. The current-flow path of the proposed converter for each stage is depicted in Fig. 2. Some typical waveforms under continuous conduction mode (CCM) operation are illustrated in Fig. 3. The operating stages are explained as follows.

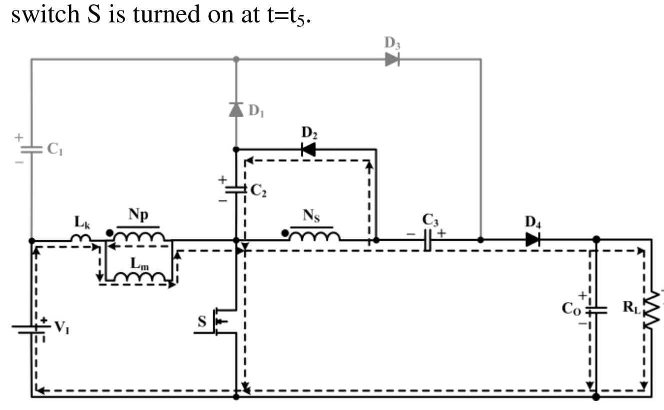
1) *Stage I [$t_0<t<t_1$ see Fig. 2(a)]:* In this stage, switch S is turned on. Also, diodes D_2 and D_4 are turned on and diodes D_1, D_3 are turned off. The DC source (V_I) magnetizes L_m through S. The secondary-side of the coupled inductor is in parallel with capacitor C_2 using diode D_2. As the current of the leakage inductor L_k increases linearly, the secondary-side current of the coupled inductor (i_S) decreases linearly. The required energy of load (R_L) is supplied by the output capacitor C_O. This interval ends when the secondary-side current of the coupled inductor becomes zero at $t=t_1$.

2) *Stage II [$t_1<t<t_2$ see Fig. 2(b)]:* In this stage, switch S and diode D_3 are turned on and diodes D_1, D_2 and D_4 are turned off. The DC source V_I magnetizes L_m through switch S. So, the current of the leakage inductor L_k and magnetizing inductor L_m increase linearly. The capacitor C_3 is charged by dc source V_I, clamp capacitor and the secondary-side of the coupled inductor. Output capacitor C_O supplies the demanded energy of the load R_L. This interval ends when switch (S) is turned off at $t=t_2$.

3) *Stage III [$t_2<t<t_3$ see Fig. 2(c)]:* In this stage, switch S is turned off. Diodes D_1 and D_3 are turned on and diodes D_2 and D_4 are turned off. The clamp capacitor C_1 is charged by the stored energy in capacitor C_2 and the energies of leakage inductor L_k and magnetizing inductor L_m. The currents of the secondary-side of the coupled inductor (i_S) and the leakage inductor are increased and decreased respectively. The capacitor C_3 is still charged through D_3. Output capacitor C_O supplies the energy to load R_L. This interval ends when i_{Lk} is equal toi_{Lm} at $t=t_3$.

4) *Stage IV [$t_3<t<t_4$ see Fig. 2(d)]:* In this stage, S is turned off. Diodes D_1 and D_4 are turned on and diodes D_2 and D_3 are turned off. The clamp capacitor C_1 is charged by the capacitor C_2 and the energies of leakage inductor L_k and magnetizing inductor L_m. The currents of the leakage inductor L_k and magnetizing inductor L_m decrease linearly. Also, a part of the energy stored in L_m is transferred to the secondary side of the coupled inductor. The dc source V_I, capacitor C_3 and both sides of the coupled inductor charge output capacitor and provide energy to the load R_L. This interval ends when diode D_1 is turned off at $t=t_4$.

5) *Stage V [$t_4<t<t_5$ see Fig. 2(e)]:* In this stage, S is turned off. Diodes D_2 and D_4 are turned on and diodes D_1 and D_3 are turned off. The currents of the leakage inductor L_k and magnetizing inductor L_m decrease linearly. Apart of stored energy in L_m is transferred to the secondary side of the coupled inductor in order to charge the capacitor C_2 through diode D_2. In this interval the DC input voltage V_I and stored energy in the capacitor C_3 and inductances of both sides of the coupled inductor charge the output capacitor C_o and provide the demand energy of the load R_L. This interval ends when switch S is turned on at $t=t_5$.



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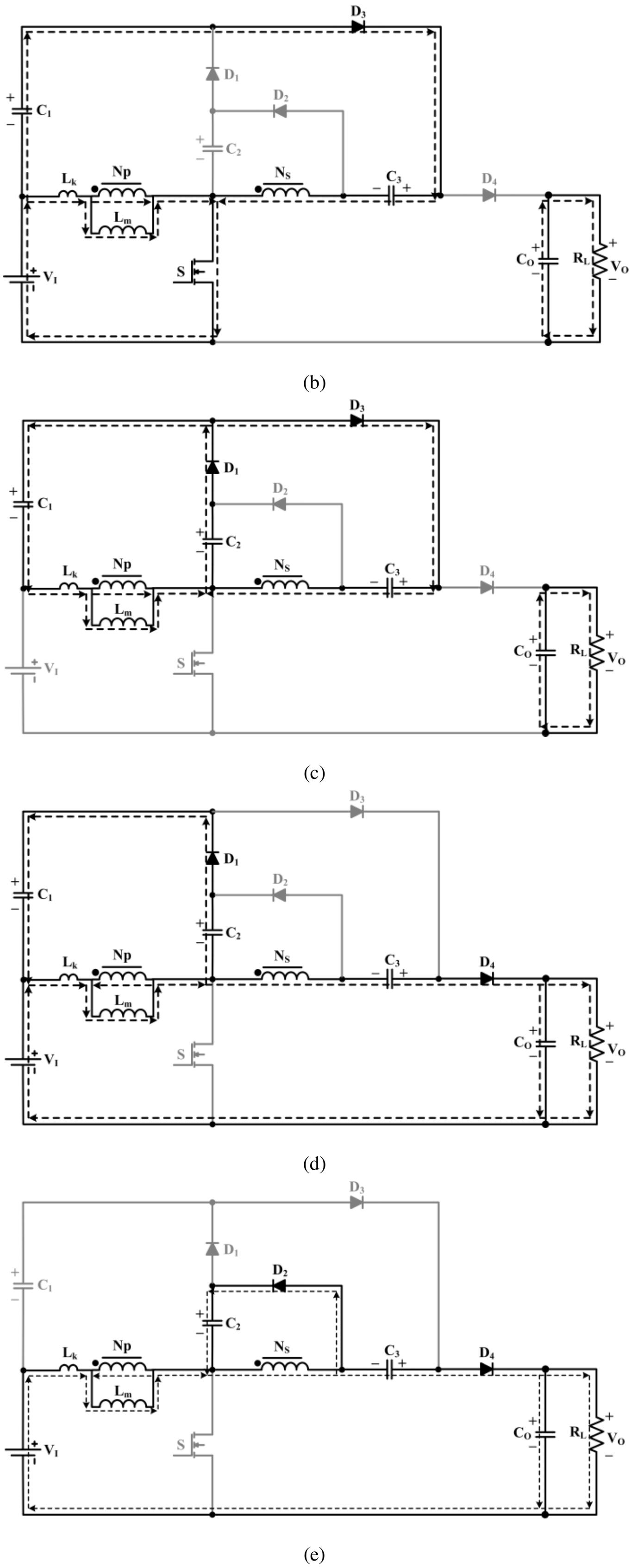

Fig. 2. Current-flow path of operating modes during one switching period at CCM operation. (a) Mode I. (b) Mode II. (c) Mode III. (d) Mode IV. (e) Mode V.

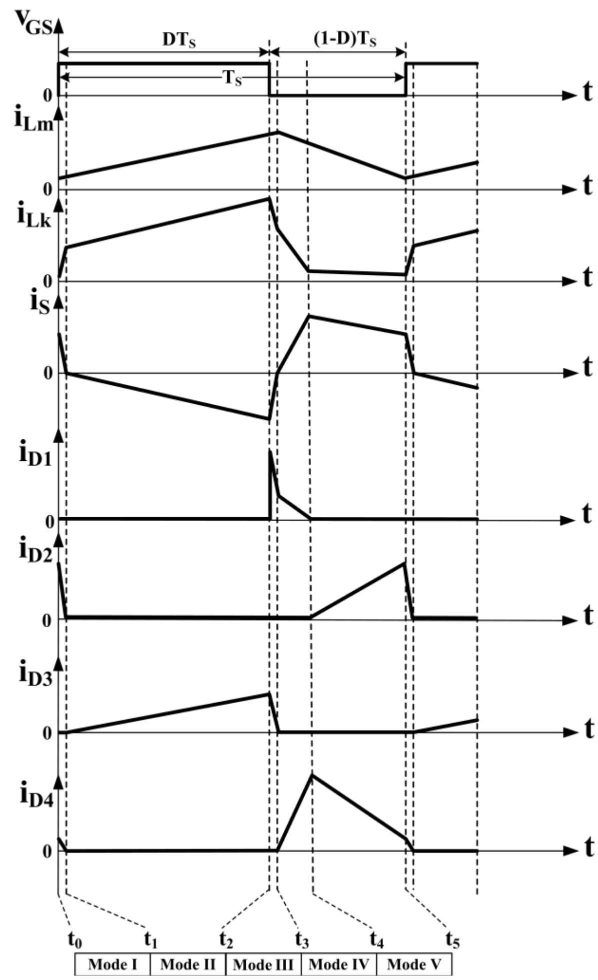

Fig. 3. Some typical waveforms of the proposed converter at CCM operation.

III. Steady-state Analysis of The Proposed Converter

A. CCM Operation

To simplify the steady-state analysis, only stages II, IV and V are considered since these stages are sufficiently large in comparison with stages I and III.

During stage II, L_k and L_m is charged by dc source V_I. Therefore, the following equation can be written according to Fig. 2(b):

$$V_{Lm} = kV_I \tag{1}$$

Where k is the coupling coefficient of coupled inductor which equals to $L_m/(L_m+L_k)$. Capacitor C_3 is charged by clamp capacitor C_1, dc source (V_I) and the secondary-side of the coupled inductor. The voltage across the capacitor C_3 can be expressed by:

$$V_{C3} = V_{C1} + (kn+1)V_I \tag{2}$$

Where n is the turn ratio of coupled inductor which is equal to N_S /N_P. As shown in Fig. 2(d), during stage IV, L_k and L_m demagnetize to the clamp capacitor C_1 with the help of capacitor C_2. Hence, the voltage across L_m can be written as:

$$V_{Lm} = k(V_{C2} - V_{C1}) \tag{3}$$

Also, the output voltage can be formulated based on Fig.

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2(d):

$$V_O = V_I + V_{C3} + (kn+1)(V_{C1} - V_{C2}) \tag{4}$$

According to Fig. 2(e), in the time interval of stage V, the voltage across L_m can be expressed by:

$$V_{Lm} = \frac{-V_{C2}}{n} \tag{5}$$

Moreover, the output voltage is derived as:

$$V_O = V_I + V_{C3} + (\frac{1}{kn}+1)V_{C2} \tag{6}$$

According to aforementioned assumption, the output capacitor voltage is constant during one switching period. Therefore, by equalization of (4) and (6), the following equation is derived as:

$$V_{C1} = \frac{kn+1}{kn}V_{C2} \tag{7}$$

Using the volt-second balance principle on L_m and equations (1), (3), (5) and (7), the voltages across capacitors C_1 and C_2 is obtained as:

$$V_{C1} = \frac{(kn+1)D}{1-D}V_I \tag{8}$$

$$V_{C2} = \frac{knD}{1-D}V_I \tag{9}$$

Substituting (8) into (2), yields:

$$V_{C3} = \frac{kn+1}{1-D}V_I \tag{10}$$

Substituting (9) and (10) into (6), the voltage gain is achieved as:

$$M_{CCM} = \frac{2+kn+knD}{1-D}V_I \tag{11}$$

Fig. 4 shows the variations of the voltage gain versus the duty ratio with different coupling coefficients of the coupled inductor. It can be seen that the coupling coefficient is not very effective on the voltage gain. When k equals 1, the ideal voltage gain is obtained as:

$$M_{CCM} = \frac{2+n+nD}{1-D}V_I \tag{12}$$

The voltage gain versus duty ratio of the proposed converter and the converters proposed in [25], [29] and [30] under CCM operation with k=1 and n=2 are depicted in Fig. 5.As it is shown n Fig. 5 the proposed converter has higher voltage transfer gain in comparison with other converters. Also, the voltage transfer gain of the presented converter is higher than the converter presented in [27]. However, in comparison with the presented converter, an additional diode, an extra capacitor and a multi-winding coupled inductor is utilized in the converter presented in [27].

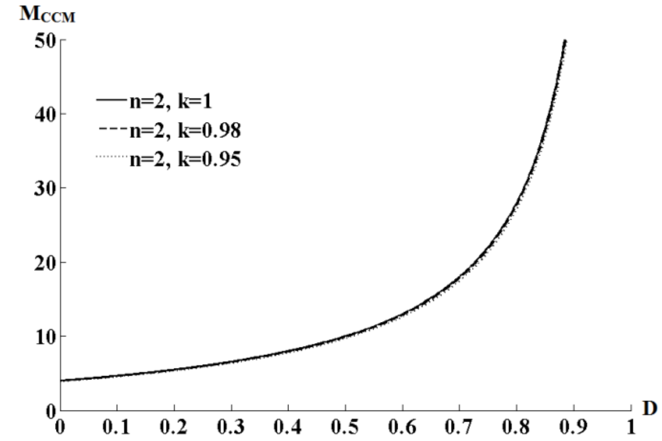

Fig. 4. Voltage gain versus duty ratio under various coupling coefficients of the coupled inductor.

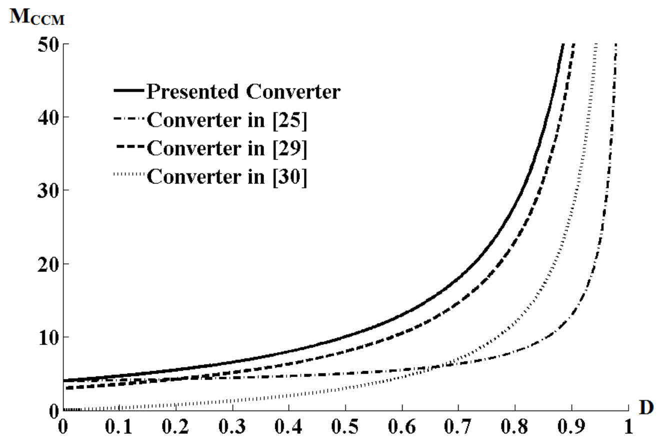

Fig. 5. Voltage gain versus duty ratio of the proposed converter, the converters in [25], [29] and [30] at CCM.

Based on the description of the operating modes, the voltage stresses on the active switch S and diodes D_1, D_2, D_3, and D_4 are expressed as:

$$V_{DS} = V_{D1} = \frac{1}{1-D}V_I = \frac{1}{2+2n}(V_O + nV_I) \tag{13}$$

$$V_{D2} = \frac{n}{1-D}V_I = \frac{n}{2+2n}(V_O + nV_I) \tag{14}$$

$$V_{D3} = V_{D4} = \frac{1+n}{1-D}V_I = \frac{1}{2}(V_O + nV_I) \tag{15}$$

According to Fig. 2, the average value of input current can be achieved as follows when switch is turned on/off:

$$I_{in(on)} = (n+1)I_{D3} + I_{Lm} \tag{16}$$

$$I_{in(off)} = I_O \tag{17}$$

From (16) and (17), the average current value of magnetizing inductor can be obtained as follow:

$$I_{Lm} = \frac{(M_{CCM} - 2 - n)I_O}{D} = \frac{2(n+1)}{1-D}I_O \tag{18}$$

The integral form of the current equation of magnetizing inductor can be written as:

$$i_{Lm}(t) = i_{Lm}(t_0) + \frac{1}{L_m}\int_{t_0}^{t} v_{Lm}(\tau)d\tau \tag{19}$$

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Substituting (16) into (19) and for k=1, t=DT and t_0=0, yielding:

$$\Delta i_{Lm} = \frac{DV_{in}}{L_m f_S} \tag{20}$$

According to Fig. 3 and applying the ampere-second balance principle on capacitors, the average current values of diodes are equal to I_O. Therefore, the peak values of diodes D_3 and D_4 can be obtained as:

$$i_{D3(peak)} = \frac{2I_O}{D} \tag{21}$$

$$i_{D4(peak)} = \frac{2I_O}{1-D} \tag{22}$$

$$i_{S(peak)} = i_{D1(peak)} = \left(\frac{2+n+nD}{D(1-D)}\right)I_O + \frac{DV_{in}}{L_m f_S} \tag{23}$$

Neglecting modes I and III, the time interval of modes IV and V are given as:

$$d_4 = \frac{2I_O}{i_{D1(peak)}} = \frac{1-D}{n+1} \tag{24}$$

$$1-D-d_4 = d_5 \tag{25}$$

From equation (25), the peak value of diode D_2 is obtained as:

$$i_{D2(peak)} = \frac{2(n+1)I_O}{n(1-D)} \tag{26}$$

B. Boundary Conduction mode (BCM) Operation

Similar to the analysis done in the former section, the voltage conversion ratio of the presented converter in discontinuous conduction mode (DCM) can be obtained as follows:

$$M_{DCM} = \frac{V_O}{V_I} = \frac{n+2+\sqrt{(n+2)^2 + \frac{D^2}{\tau_{Lm}}}}{2} \tag{27}$$

If the proposed converter is operated in BCM, the voltage gain in the CCM will be equal to its voltage gain in the DCM operation. From (12) and (27), the boundary normalized magnetizing-inductor time constant τ_{LmB} can be formulated as:

$$\tau_{Lm,B} = \frac{D(1-D)^2}{8(n^2(1+D)+n(3+D)+1)} \tag{28}$$

The normalized magnetizing-inductor time constant τ_{Lm}can be written as:

$$\tau_{Lm} = \frac{f_s L_m}{R_L} \tag{29}$$

Fig. 6 shows the curve of τ_{LmB}. If $\tau_{Lm}$is larger than τ_{LmB}, the proposed converter is operated under CCM. Fig. 7 shows the Comparison of τ_{LmB} of the presented converter with converters in [28], [29] with respect to the duty cycle and the conversion ratio. As it is shown in Fig. 7, the CCM region of the presented converter is wider. Also, the CCM region of the presented converter is wider than the converter presented in [27]. Therefore, the presented converter requires a smaller magnetizing inductance to assure the CCM operation of the converter.

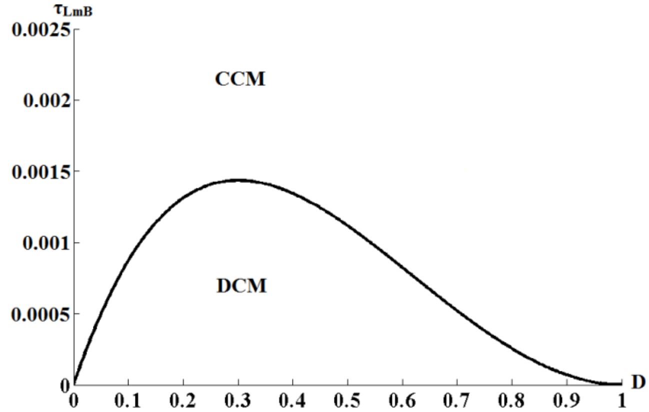
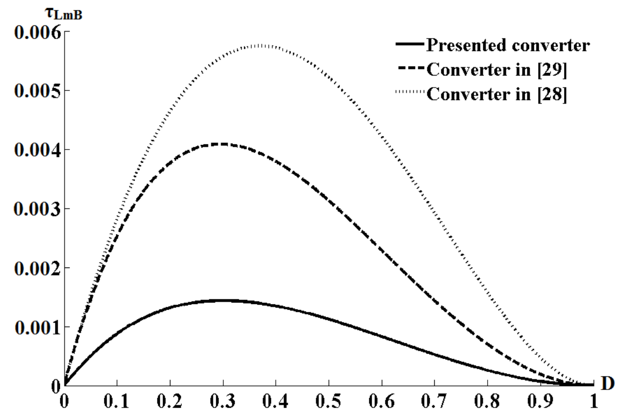
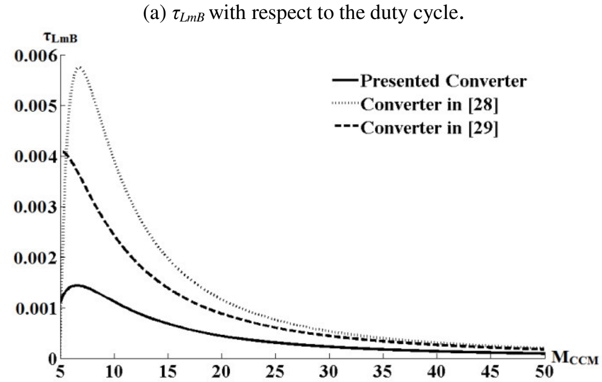


Fig. 6. Boundary condition of the proposed converter under n=2.



(a) τ_{LmB} with respect to the duty cycle.



(b) τ_{LmB} with respect to the conversion ratio.

Fig. 7. Comparison of τ_{LmB} of the presented converter with converters in [28], [29].

IV. Capacitors and Inductance Calculation

The magnetizing inductance of the coupled inductor is designed according to (28) and (29). To assure the CCM operation of the presented converter, the value of τ_{Lm} must be more than $\tau_{Lm,B}$. Therefore, the minimum value of the magnetizing inductance can be calculated as follows:

$$L_{m_{min}} = \frac{D(1-D)^2 R_L}{8 f_S (n^2(1+D)+n(3+D)+1)} \tag{30}$$

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According to (30), the magnetizing inductance should be more than 148μH. A coupled inductor with the magnetizing inductance of the 300μH is employed to guarantee the CCM operation of the implemented converter.

In order to design the size of the capacitors, it should be followed four conditions regarding the ripple in the output voltage. The conditions are ripple of the capacitor current, ripple due to the equivalent series resistance (ESR) of the capacitor, ripple due to the equivalent series inductance (ESL) of the capacitor, and the hold-up time requirement for load step response which the last condition is for the output capacitor. First, the design is started by considering only the first condition which ESRs and ESLs are not known before selecting the capacitor. Then, ESRs and ESLs are obtained from the capacitors' datasheets. The total output voltage ripple is checked to make sure that it is below the admissible value by considering ESRs and ESLs. In addition, the ripple of the capacitor currents are calculated and compared to the value mentioned in datasheet to make sure that the selected capacitors are in consistent with the practical conditions. In order to calculate the voltage ripple of a capacitor ESR and ESL, the following equation is used.

$$V_C(t) = V_C(\mathrm{t}_0) + \frac{1}{C}\int_{t_0}^{t} i(t)dt$$

(31)

Since the average currents through capacitors C_1, C_2, C_3 and C_O are zero under steady state, the average current values of diodes are equal to I_O. Therefore, according to the CCM operation modes shown in Fig. 2 and (31), the voltage ripple of all capacitors can be given as follows:

$$\Delta V_{C1,2,3} = \frac{V_O}{R_L C} \quad , \quad \Delta V_{CO} = \frac{DV_O}{R_L C_O f_S} \tag{32}$$

The peak-to-peak voltage across ESR of a capacitor can also be considered as follows:

$$\Delta V_C^{ESR} = r_C \Delta I_C \tag{33}$$

According to equations (21)-(23), (26) and (33), the peak-to-peak voltages across the capacitors' ESR are expressed below:

$$\begin{aligned}
\Delta V_{C1}^{ESR} &= r_{C1}\left(\left(\frac{4+n+(n-2)D}{D(1-D)}\right)I_O + \frac{DV_{in}}{L_m f_S}\right)\\
\Delta V_{C2}^{ESR} &= r_{C2}\left(\left(\frac{2+n+nD+\dfrac{2D(n+1)}{n}}{D(1-D)}\right)I_O + \frac{DV_{in}}{L_m f_S}\right)\\
\Delta V_{C3}^{ESR} &= r_{C3}\frac{2I_O}{D(1-D)}\\
\Delta V_{CO}^{ESR} &= r_{CO}\frac{2I_O}{1-D}
\end{aligned} \tag{34}$$

The peak-to-peak voltage across ESL of a capacitor can also be considered as follows:

$$\Delta V_C^{ESL} = L_C \frac{di_C}{dt} \tag{35}$$

According to equations (21)-(23), (26) and (35), the peak-to-peak voltages across ESL of the capacitors are expressed below:

$$\begin{aligned}
\Delta V_{C1}^{ESL} &= L_{C1}\left(\frac{(n+1)\left(\left(\dfrac{2+n+nD}{D(1-D)}\right)I_O + \dfrac{DV_{in}}{L_m f_S}\right)}{(1-D)T_S} + \frac{2I_O}{D^2 T_S}\right)\\
\Delta V_{C2}^{ESL} &= L_{C2}\left(\frac{(n+1)\left(\left(\dfrac{2+n+nD}{D(1-D)}\right)I_O + \dfrac{DV_{in}}{L_m f_S}\right)}{(1-D)T_S} + \frac{2(n+1)^2 I_O}{\mathrm{n}^2(1-D)^2 T_S}\right)\\
\Delta V_{C3}^{ESL} &= L_{C3}\left(\frac{2I_O}{(1-D)^2 T_S} + \frac{2I_O}{D^2 T_S}\right)\\
\Delta V_{CO}^{ESL} &= L_{CO}\left(\frac{2I_O}{(1-D)^2 T_S}\right)
\end{aligned} \tag{36}$$

By imposing a certain ripple value, the sizes of the capacitors are calculated using equation (32). Then, by knowing ESRs and ESLs of the chosen capacitors, the total voltage ripple, $\Delta V_C + \Delta V_C^{ESR} + \Delta V_C^{ESL}$, have to be checked to be less than the desired proportion of capacitor voltages. In addition, the root-mean-square (rms) value of capacitor currents should also be calculated to make sure that they meet the values mentioned in the datasheet. Therefore, the rms values of capacitor currents are as follows:

$$\begin{aligned}
i_{C1rms} &= \sqrt{\left(\left(\left(\frac{2+n+nD}{D(1-D)}\right)I_o + \frac{DV_{in}}{L_m f_s}\right)\sqrt{\frac{3(1-D)}{1+n}}\right)^2 + \left(\frac{2I_o}{D}\sqrt{\frac{D}{3}}\right)^2}\\
i_{C2rms} &= \sqrt{\left(\left(\left(\frac{2+n+nD}{D(1-D)}\right)I_o + \frac{DV_{in}}{L_m f_s}\right)\sqrt{\frac{3(1-D)}{1+n}}\right)^2 + \left(\frac{2(n+1)I_o}{\mathrm{n}(1-D)}\sqrt{\frac{3(1-D)\mathrm{n}}{1+n}}\right)^2}\\
i_{C3rms} &= I_O\sqrt{\left(\frac{2}{1-D}\sqrt{\frac{1-D}{3}}\right)^2 + \left(\frac{2}{D}\sqrt{\frac{D}{3}}\right)^2}\\
i_{COrms} &= I_O\sqrt{\frac{1+D^2}{3(1-D)}}
\end{aligned} \tag{37}$$

An important condition in the design of the output capacitor in any converter is the hold-up time requirement for step-load response. A load variation, ΔI_{out}, in the load current causes a load voltage change, ΔV_{CO}. It takes a short nonzero time, τ, until the feedback loop responds to bring back the load voltage to its steady-state value. According to [31], this duration is usually approximated as $1/(0.1f_s)$. During the time τ, the capacitor must hold the load voltage, such that ΔV_{CO} remains under the acceptable ripple value, usually 1% of V_{out}. This means that the capacitor value has to be at least:

$$C_{O\min} = \frac{\Delta I_{out}}{0.01\ V_{out}}\tau \tag{38}$$

The sizes of the capacitors for the implemented circuit which are mentioned in Table 1 satisfy the all conditions explained above.

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V. Experimental Results

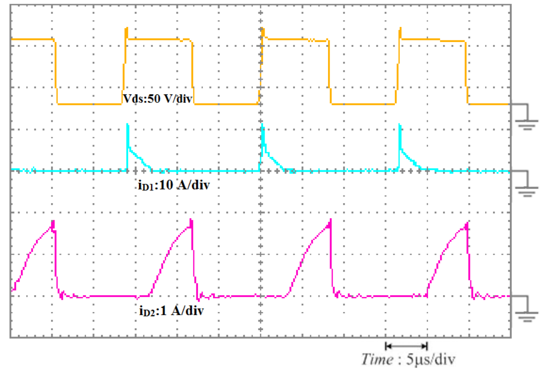
The performance of the presented converter is assessed using the prototype circuit implemented in the laboratory. The specifications of the implemented circuit are given in Table 1.

The experimental results are shown in Fig. 8 under load 300W. The results verify the analysis of the steady state operation. The voltage on the switch (V_{DS}) during the turn-off state is clamped to about 80V. Therefore, a low-voltage-rated switch can be used to improve the efficiency of the presented converter. Fig. 8(a) shows that the energy stored in the leakage inductance is recycled to capacitor C_1 through diode D_1. Fig. 8(e), (f) depict the voltage stresses on the main switch and diodes. Also, Fig. 8(d) shows the voltages on capacitors C_1, C_2, C_3 and C_O which are in consistency with (8)-(11). The current waveforms of the diodes, switches and the coupled inductor (i_{LK}) shown in Fig. 8(a)-(c) validate the analysis and the feasibility of the proposed converter. The input current waveform with and without an input filter is also shown in Fig. 8(g).The input current ripple is as much as other proposed high step-up converters such as the converters in [27] - [29]. However, as it is shown in Fig. 8(g) (i_{Source}), a low pass filter can be used to reduce the input current ripple.

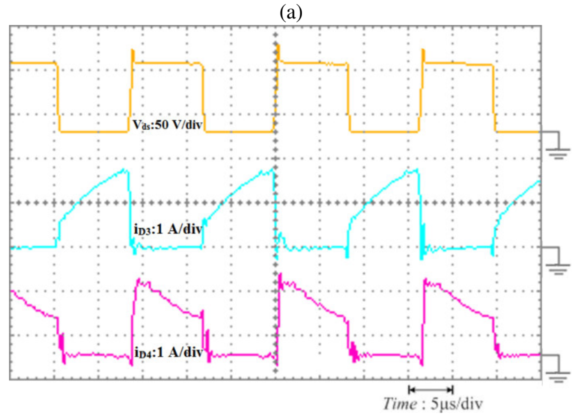
The experimental conversion efficiency of the presented converter is given in Fig. 9. The peak value of efficiency is 96.9% which is achieved at P_O=200W. The efficiency of the presented converter at full load P_O=300W is 96%. The results show the high conversion efficiency of the presented converter.

TABLE I
SPECIFICATIONS OF THE IMPLEMENTED PROTOTYPE

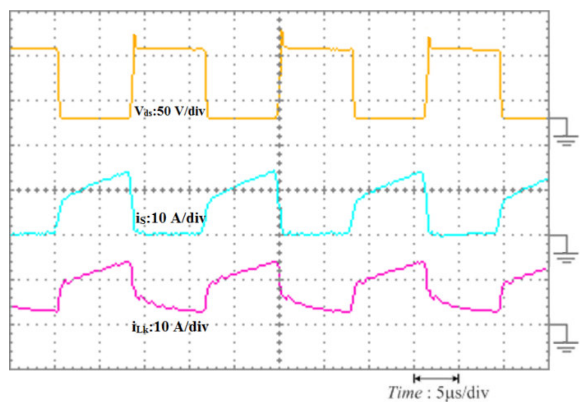
Specifications	Values
Input DC voltage	V_{in}=40 V
Output DC voltage	V_{out}=400 V
Switching frequency	F=60 kHz
Fast Diodes D_1, D_2, D_3, D_4	U1560
Coupled inductor	L_K: 1 µH, L_m: 300 µH
Capacitors C_1, C_2, C_3, C_o	47, 47, 100, 220 µF
Load	300 W
Power Switch (MOSFET)	IRFP260



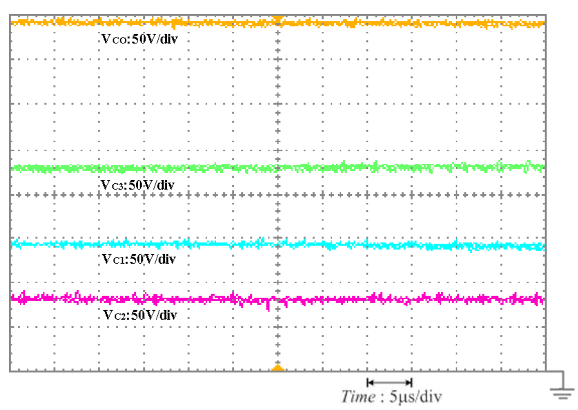
(a)



(b)



(c)



(d)

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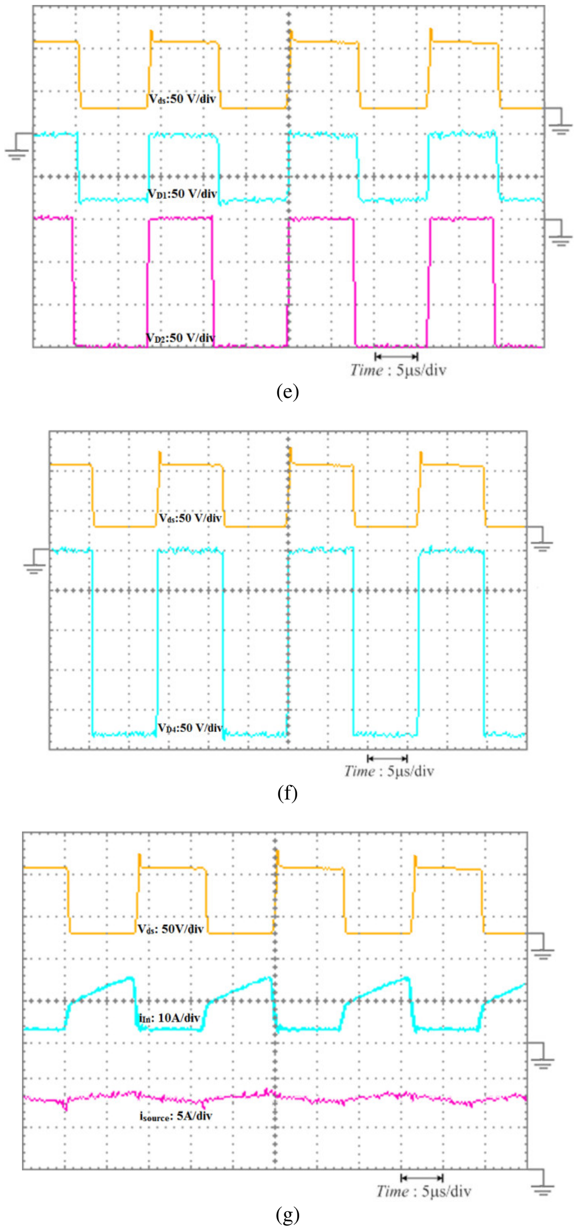

Fig. 8. Experimental results under load 300 W.

The experimental conversion efficiency of the presented converter is given in Fig. 9. The peak value of efficiency is 96.9% which is achieved at P_O=200W. The efficiency of the presented converter at full load P_O=300W is 96%. The results show the high conversion efficiency of the presented converter.

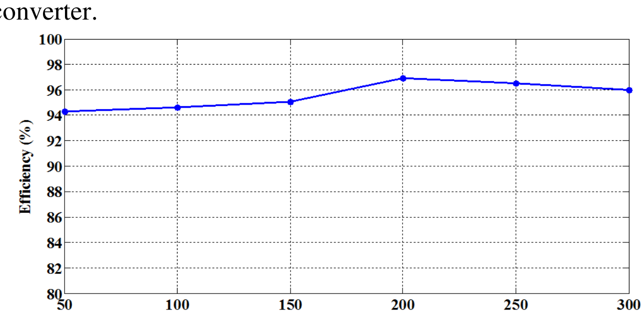

Fig. 9. Experimental conversion efficiency.

VI. Conclusion

This paper presents a new high step-up DC/DC converter for Renewable Energy Applications. The suggested converter is suitable for DG systems based on renewable energy sources which require high step-up voltage transfer gain. The energy stored in the leakage inductance is recycled to improve the performance of the presented converter. Furthermore, voltage stress on the main power switch is reduced. Therefore, a switch with a low on-state resistance can be chosen. The steady-state operation of the converter has been analyzed in detail. Also, the boundary condition has been obtained. Finally, a hardware prototype is implemented which converts the 40-V input voltage into 400-V output voltage. The results prove the feasibility of the presented converter.

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