A Quasi-Unipolar SPWM Full-Bridge Transformerless PV Grid-Connected Inverter with Constant Common-Mode Voltage

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***Abstract*—The unipolar sinusoidal pulsewidth modulation (SPWM) full-bridge transformerless photovoltaic (PV) inverter with ac bypass brings low conduction loss and low leakage current. In order to better eliminate the leakage current induced by the common-mode voltage, the clamping technology can be adopted to hold the common-mode voltage on a constant value in the freewheeling period. A full-bridge inverter topology with constant common-mode voltage (FB-CCV) has been derived and proposed in this paper, two unidirectional freewheeling branches are added into the ac side of the FB-CCV, and the split structure of the proposed freewheeling branches does not lead itself to the reverse-recovery issues for the freewheeling power switches and as such superjunction MOSFETs can be utilized without any efficiency penalty. The passive clamping branches consist of a capacitor divider and two diodes, is added into the dc side of the FB-CCV, therefore, the weakness of active damping branch has been overcome, and the better clamping performance has been achieved in the freewheeling period. In the dead time between the main switches and the freewheeling switches, the antiparallel diodes of diagonal main switches of the FB-CCV form the freewheeling path to clamp the common-mode voltage at a constant value, and a quasi-unipolar SPWM strategy is presented. The operation principle, differential-mode and common-mode characteristics of the FB-CCV, Heric, H6 and HB-ZVR topologies are analyzed and compared in detail. Finally, the viability of the FB-CCV is verified by a universal prototype inverter rated at 5 kW.**

***Index Terms*—Full-bridge inverter; Quasi-unipolar SPWM (qSPWM); Common-mode voltage; Passive clamping**

I. INTRODUCTION

TRANSFORMERLESS grid-connected inverters have a lot of advantages such as higher efficiency, smaller size, lighter weight, lower cost and so on. [1-12]. The unipolar sinusoidal pulsewidth modulation (SPWM) full-bridge inverter has received extensive attentions owing to its excellent differential-mode characteristics such as higher dc voltage utilization, smaller current ripple in the filter inductor, and higher processing efficiency [13]. However, the common-mode leakage current induced by the modulation strategy is brought in electrical systems [14-21].

In order to improve the common-mode performance of the unipolar SPWM full-bridge transformerless grid-connected inverter, a lot of in-depth research works, where the new freewheeling paths are constructed to separate the PV array from the grid in the freewheeling period, have been done in [22-31]. Several methods can be divided into the ac bypass [25-27] and the dc bypass [28-31]. The goal is to structure a simple, efficient, and reliable transformerless inverter topology for transformaerless photovoltaic (PV) grid-connected application. Based on the common-mode equivalent model of the full-bridge inverter derived in [21], it is necessary that the potential of the freewheeling path is clamped to a half input voltage in the freewheeling period instead of only disconnecting the PV array from the grid. Depending on this rule, the switching frequency common-mode voltage can be completely avoided in the unipolar SPWM full-bridge inverter. The topologies in [27], [29], and [30], are complying with the aforementioned conclusion; however, their clamping ability is different. In [27] (the topology is shown in Fig. 1(a), and is named as HB-ZVR), if the potential of the freewheeling path rises, it can be clamped, while if the potential falls, it cannot be clamped. In [29], Gonzalez et al. have brought a diode clamping branch into the input voltage side (shown in Fig. 1(b), named as H6 in this paper), and the potential of the freewheeling path can be seamlessly clamped to a constant voltage in the freewheeling period. In [30], when the potential of the freewheeling path falls, it can be seamlessly clamped, however, when the potential rises, it is not clamped effectively during the dead time between the high frequency main switch and the clamping one. Apparently, the leakage current suppression performance in these three kinds of topologies is different due to the clamping ability. The H6 topology has the best performance about leakage current suppression in existing single-phase full-bridge transformerlsee topologies [30].

The losses of power devices in the topologies that are illustrated in [25], [29], [30], have been calculated in different switching frequencies in [20]. It can be seen that the conduction losses (including freewheeling losses) have a large

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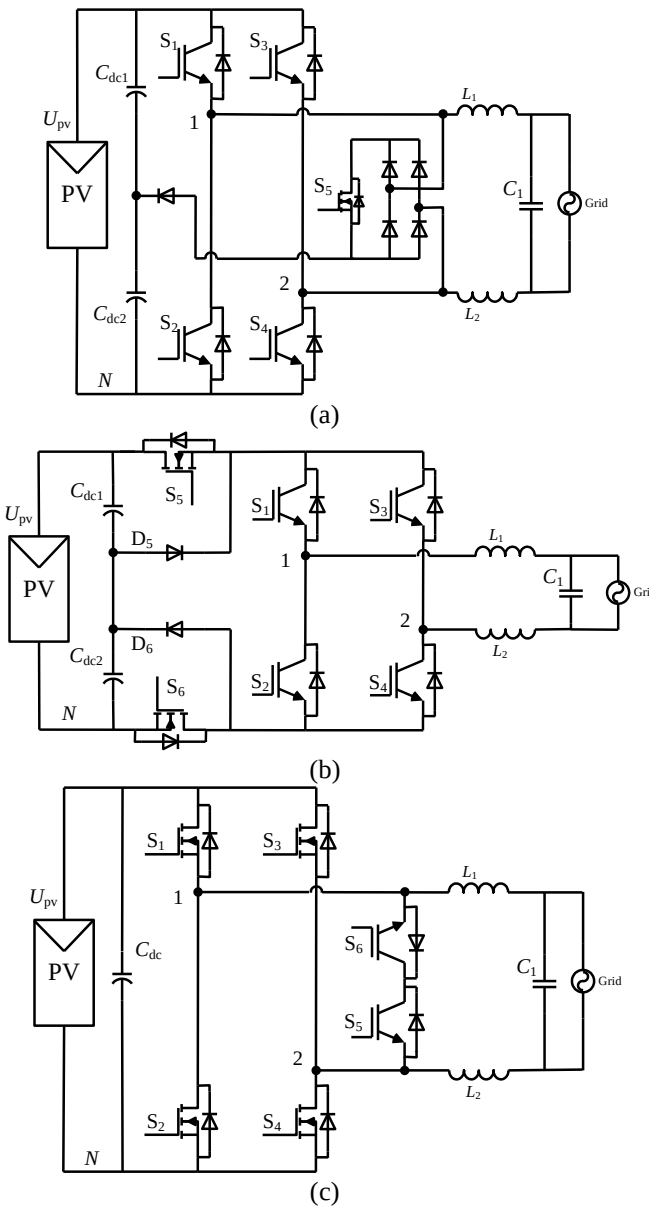

Fig. 1. Typical transformerless inverter topologies. (a) HB-ZVR topology. (b) H6 topology. (c) Heric topology.

proportion in the total losses, therefore, reducing the conduction losses is beneficial to improve the efficiency of the inverter continually. Referring to Fig. 1 (c), the topology in [25] (named as Heric) has the minimum conduction losses and the total losses, and the reason is that the output current flows through only two power switches in the power processing period and the freewheeling period, respectively. The output current of other topologies flows through three or even four power devices at least [26-31]. Therefore, the Heric topology has the least losses of power devices in existing hard-switching topologies of the single-phase full-bridge transformerless PV grid-connected inverter [30].

From the aforementioned analysis, two rules can be concluded to realize a better tradeoff between the differential-mode and common-mode characteristics of the single-phase full-bridge transformerless grid-connected inverter: 1) Improve the leakage current suppression performance based on the Heric topology with the highest hard-switching conversion efficiency; or 2) Improve the conversion efficiency based on the H6 topology with the best leakage current suppression.

This paper focuses on improving the leakage current suppression performance of the Heric topology by using passive clamping technology, according to rule 1). First, a full-bridge inverter topology with constant common-mode voltage (FB-CCV) is proposed in this paper. Compared with the Heric topology [25], the freewheeling path is reconstructed in the ac side, and a passive clamping branch is added into the dc side to clamp the potential of the freewheeling path in the freewheeling period. Under the effect of the proposed modulation strategy, the inductor current flows through the antiparallel diodes of diagonal main switches of the FB-CCV during the dead time between the main switches and the freewheeling switches, and this stage is consistent with the freewheeling mode of the bipolar SPWM full-bridge inverter, which guarantees that the common-mode voltage is a constant value in the dead time. Until the end of the dead time, the freewheeling path starts to provide the zero-vector freewheeling, and this stage is same with the freewheeling mode of the unipolar SPWM full-bridge inverter. By running the combined operation modes, the common-mode voltage is held on a constant value in whole switching period. For convenience, the novel modulation strategy is named as quasi-unipolar SPWM (qSPWM).

This paper is organized as follows. The second section presents the circuit structure and operation principle of the FB-CCV. The differential-mode and common-mode characteristics of the FB-CCV are introduced in Section III. The experimental results are shown in Section IV to explore the performance of the FB-CCV. Section V summarizes the conclusions drawn from the investigation.

II. Structure and Operation Principle

A. Construction of the FB-CCV

In order to guarantee that the common-mode voltage of the Heric is on a constant value in the freewheeling period, the procedure of deriving the freewheeling branches and passive clamping branches will be demonstrated in the following how a Heric topology, as shown in Fig. 1(c), can be transformed to a FB-CCV topology, as shown in Fig. 3(a).

Step 1) First, the bidirectional freewheeling branches are extracted from the Heric topology, as shown in Fig. 2(a). Separate the bidirectional branches to form two unidirectional branches shown in Fig. 2(b).

Step 2) Next, the positions of S_5 and D_5 are exchanged in the unidirectional branch B, as shown in Fig. 2(c).

Step 3) Finally, find or build a clamping voltage source in the full-bridge inverter (for example, point 3 in Fig. 2(d)), than introduce two clamping diodes D_7 and D_8 into the inverter to connect the center points of the two unidirectional branches to the clamping voltage source. The direction of the clamping diodes can be determined using the back to back rule of D5 and D6, as shown in Fig. 2(d).

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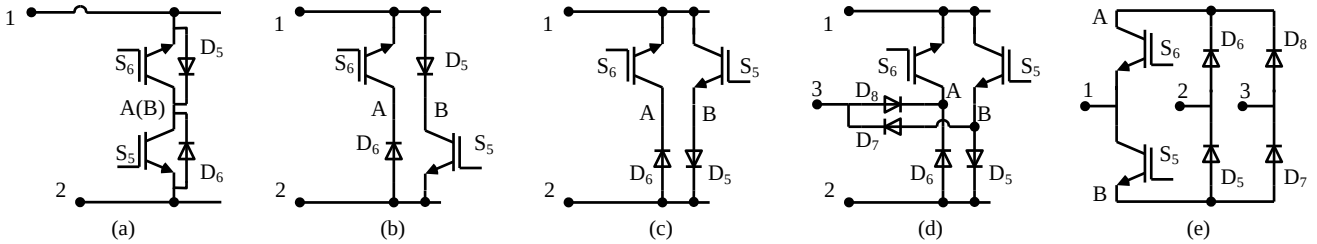

Fig. 2. Derivation of the freewheeling branches and passive clamping branches. (a) Bidirectional freewheeling branches. (b) Two unidirectional branches Ⅰ. (c) Two unidirectional branches Ⅱ. (d) Proposed freewheeling branches with passive clamping branches. (e) Bridge leg structure.

Remark: It should be mentioned that the freewheeling branches and passive clamping branches can be rearranged as bridge leg structure, as shown in Fig. 2(e). We can define that S_5 and S_6 make up the active freewheeling leg, D_5 and D_6 make up the passive freewheeling leg, and D_7 and D_8 make up the passive clamping leg.

According the aforementioned steps, the capacitors C_{dc1} and C_{dc2}, in series, are introduced into the dc side of the Heric to build the clamping voltage source, and the freewheeling branches and passive clamping branches shown in Fig. 2(d) are introduced into the Heric also, finally, the FB-CCV topology is constructed, as shown in Fig. 3(a). The drive signals of qSPWM are shown in Fig. 3(b), and the key operation waveforms of the FB-CCV with qSPWM are shown in Fig. 3(c), respectively. In the positive half period of the grid-in current, the operation style of S_1 and S_4 is in unipolar SPWM modulation, S_2 and S_3 are always off, and the switches S_5 and S_6 are complementary with the switches S_1 and S_4 with a dead time to avoid the short-circuit paths from S_1, S_5, D_5, S_4, and S_1, S_5, D_7, respectively; in the negative half period of the grid-in current, the operation style of S_2 and S_3 is in unipolar SPWM modulation, S_1 and S_4 are always off, and the switches S_5 and S_6 are complementary with the switches S_2 and S_3 with a dead time to avoid the short-circuit paths from S_3, D_6, S_6, S_2, and D_8, S_6, S_2, respectively.

In the qSPWM style, there are two freewheeling modes in the freewheeling period. One is dead-time mode, such as the time intervals [t_2, t_3] and [t_4, t_5] in Fig. 3(c); another is zero-vector mode, the time interval [t_3, t_4], as shown in Fig. 3(c) also. Especially, the potential of the zero-vector freewheeling path is defined as the potential of points 1 and 2 as shown in Fig. 3(a), and the zero-vector freewheeling path can be freely clamped to the midpoint of the input voltage (it is the point 3) through the diodes D_7 and D_8 in the zero-vector freewheeling stage.

B. Operation Principle Analysis

Before analysis, the following assumptions are given: 1) All active power devices are ideal switches with antiparallel diodes, and the power diodes are also ideal diodes without parasitic parameters; and 2) The capacitance C_{dc1} and C_{dc2} of the dc filter are large enough to be treated as constant voltage sources. Fig. 3(c) shows the key operation waveforms of the FB-CCV at the grid frequency scale, a grid period can be divided into fore states, I (u_g>0 and i_{ref}>0), II (u_g<0 and i_{ref}>0), III (u_g<0 and i_{ref}<0), and IV (u_g>0 and i_{ref}<0), respectively. Because of the similarity, only the switching modes in the positive half period

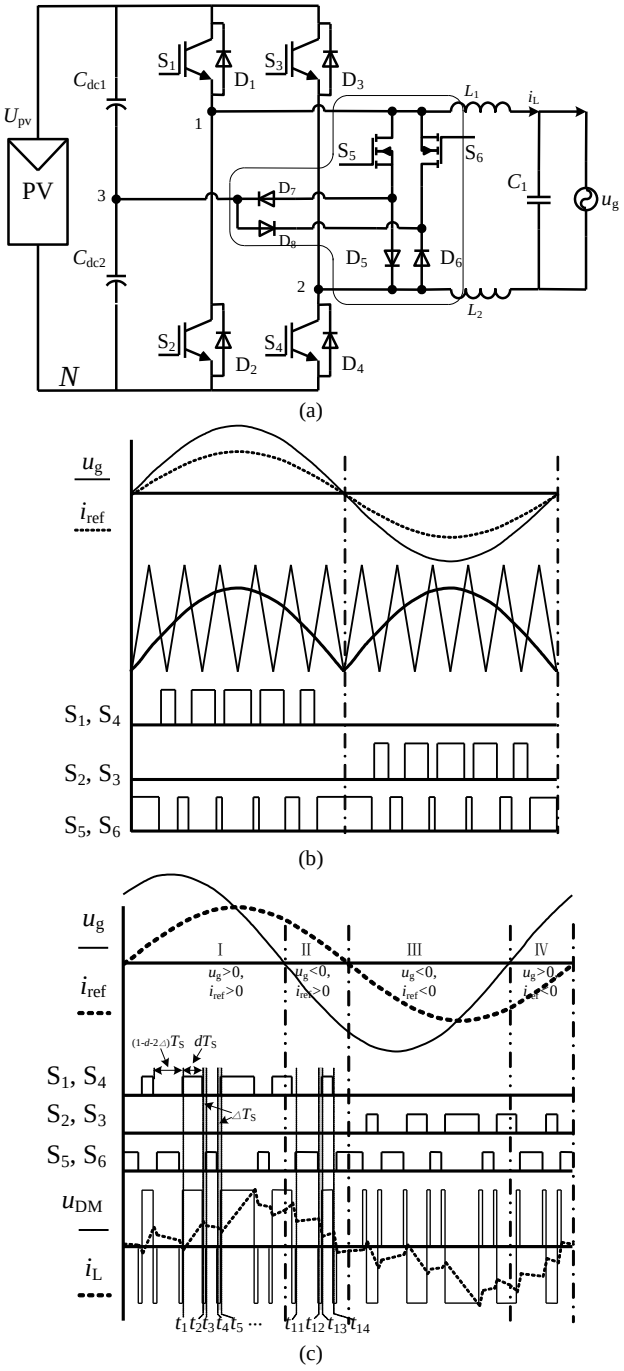

Fig. 3. Proposed transformerless PV grid-connected inverter. (a) FB-CCV topology. (b) Gate drive signal of the qSPWM with unity power factor. (c) Key operation waveforms of the FB-CCV with qSPWM.

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of the grid-in current are described in detail. In state I, there are three kinds of stages.

Stage I-1 [t_1, t_2]: Refer to Fig. 3(c) and Fig. 4(a). At t_1, the main switches S_1 and S_4 are turned on and other switches are off, the inductor current i_L=$I_L(t_1)$. In this stage, the power flows from the PV side to the grid through S_1, S_4 and filter. The inductor current i_L increases linearly until t_2, this stage is named as power mode.

$$i_L(t)-I_L(t_1)=\frac{U_{pv}-u_g}{L}(t-t_1) \tag{1}$$

$$u_{12}=U_{pv} \tag{2}$$

Stage I-2 [t_2, t_3]: Refer to Fig. 4(b). At t_2, S_1 and S_4 are turned off, and then all switches are off. This stage is called as dead-time freewheeling mode. The inductor current i_L flows into dc bus capacitor through the antiparallel diodes D_2 and D_3. The inductor current i_L reduces linearly under the effects of the PV voltage and the grid voltage,

$$i_L(t)-I_L(t_2)=\frac{-U_{pv}-u_g}{L}(t-t_2) \tag{3}$$

$$u_{12}=-U_{pv} \tag{4}$$

Stage I-3 [t_3, t_4]: Refer to Fig. 4(c). At t_3, the freewheeling switches S_5 and S_6 are turned on with the same commutation order, and other switches are off. This stage is called as zero-vector freewheeling mode. The inductor current i_L flows through the diode D_6 and the switch S_6. The inductor current i_L reduces linearly under the effect of the grid voltage,

$$i_L(t)-I_L(t_3)=\frac{-u_g}{L}(t-t_3) \tag{5}$$

$$u_{12}=0 \tag{6}$$

At t_4, S_5 and S_6 are turned off, and then all switches are off, the inverter works at the dead-time freewheeling mode again (likes stage I-2).

In state II, the grid voltage goes into negative half period, and the grid-in current still stays at positive direction.

Stage II-1 [t_{11}, t_{12}]: At t_{11}, the freewheeling switches S_5 and S_6 are turned on, and other switches are off. The direction of the grid voltage is reversed, and the inductor current i_L flows through the diode D_6 and the switch S_6, is linearly increased under the effect of the grid voltage (Fig. 4(c) can be referred as the equivalent circuit, but the bottom of the symbol of the grid is positive direction). This stage is called as the energy storage mode.

$$i_L(t)-I_L(t_{11})=\frac{|U_g|}{L}(t-t_{11}) \tag{7}$$

$$u_{12}=0 \tag{8}$$

Stage II-2 [t_{12}, t_{13}]: At t_{12}, S_5 and S_6 are turned off, and then all switches are off. The inductor current i_L flows into the dc bus capacitor through the antiparallel diodes D_2 and D_3, from the grid. The inductor current i_L reduces linearly under the effect of the difference of the PV voltage and grid voltage.

$$i_L(t)-I_L(t_{12})=\frac{-U_{pv}+|U_g|}{L}(t-t_{12}) \tag{9}$$

$$u_{12}=-U_{pv} \tag{10}$$

Stage II-3 [t_{13}, t_{14}]: At t_{13}, the main switches S_1 and S_4 are turned on and other switches are off. In this stage, the energy is stored in filter inductors through S_1, and S_4. The inductor current i_L is increased linearly until t_{14}.

$$i_L(t)-I_L(t_{13})=\frac{U_{pv}+|U_g|}{L}(t-t_{13}) \tag{11}$$

$$u_{12}=U_{pv} \tag{12}$$

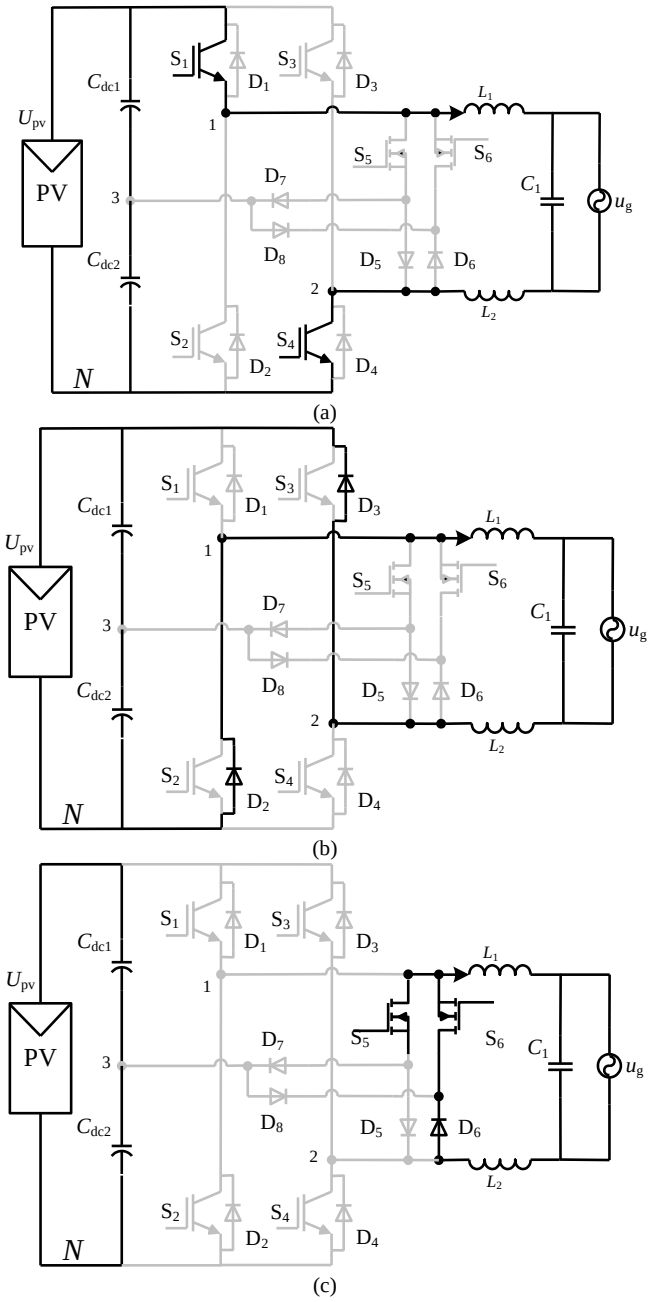

Fig. 4. Equivalent circuits in the positive half period of the grid-in current. (a) Stage 1 [t_1, t_2]. (b) Stage 2 [t_2, t_3]. (c) Stage 3 [t_3, t_4].

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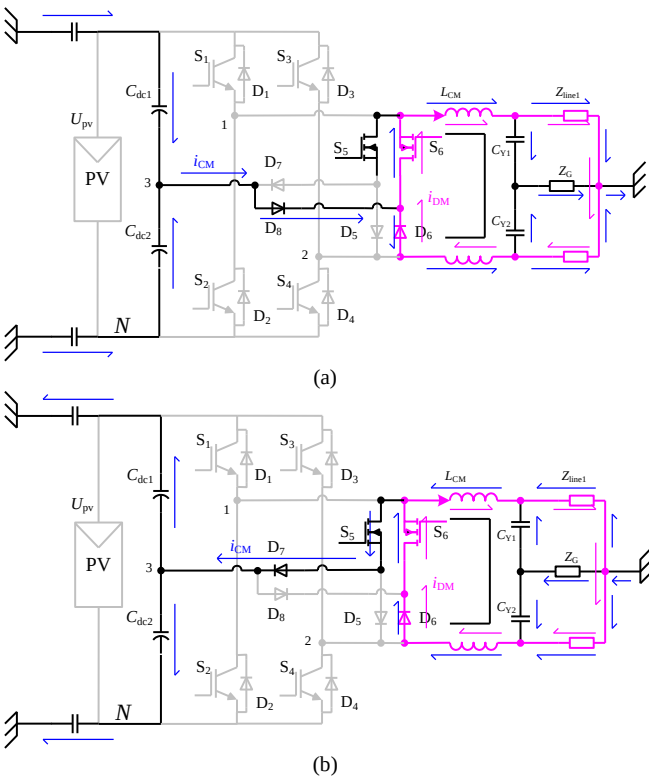

Fig. 5. Equivalent circuits in the clamped mode. (a) The potential of the zero-vector freewheeling path falls. (b) The potential of the zero-vector freewheeling path rises.

From above analysis, we can see that the auxiliary switches S_5 and S_6 run at high-frequency switching pattern. This makes it possible to have a reactive power flow that can be used to support the grid with additional services any time during the functioning of the inverter.

C. Operation Principle of the Clamping Branch

The equivalent circuits of the clamping mode are shown in Fig. 5. In the positive half period of the grid-in current, the path of the grid current (it is the differential-mode current i_{DM}) is D_6, S_6, filter, grid lines and return to D_6, in sequence. If the potential of the freewheeling path falls, the common-mode current flows through D_8, and the blue arrow represents the direction of the common-mode current i_{CM}, as shown in Fig. 5(a); when the potential of the freewheeling path rises, the common-mode current flows through D_7, and the blue arrow represents the direction of the common-mode current i_{CM}, as shown in Fig. 5(b). Obviously, in both cases, the potential of the freewheeling path can be freely clamped to $0.5*U_{PV}$. In the negative half period of the grid-in current, the clamping process is similar with the positive half period.

III. Characteristics of the Novel Inverter

A. Differential-mode characteristics

Assuming the negative terminal "N" of PV solar panels as the reference point, the midpoints "1" and "2" of the bridge legs are output terminals. According to the definition of differential-mode voltage, the differential-mode voltage v_{DM} is related to v_{1N} and v_{2N}, as shown in the following:

$$u_{DM} = u_{1N} - u_{2N} = u_{12} \tag{13}$$

Refer to Fig. 3(c), the differential-mode voltage of the FB-CCV has three kinds of levels U_{pv}, $-U_{pv}$, and 0 in each switching period, this is different with the bipolar SPWM and the unipolar SPWM. According to the switching states and the direction of the grid-in current, the differential-mode voltage can be listed in Table II.

It can be seen from the analysis of the operation modes that the qSPWM makes the commutating process of the active power devices to suffer from the full dc link voltage, and the active power devices of the Heric and H6 need to commutate only half the dc link voltage. The disadvantage will increase the turn on and off losses, likes the HB-ZVR [27]. Advantageously, the grid-in current of the FB-CCV flows through only two power devices in Stage 1, Stage 2, and Stage 3, respectively. Noteworthy, the zero-vector conduction loss of MOSFET + diode freewheeling paths of the FB-CCV is less than both of IGBT + diode freewheeling paths of the Heric and H6, and MOSFET + diode + diode freewheeling paths of the HB-ZVR. In order to improve the zero-vector conduction loss further, and hence to reduce the total power loss, a full MOSFET paralleled path is proposed to form the zero-vector freewheeling path [32], as shown in Fig. 6. We can see that two back to back MOSFETs are used to form freewheeling path, therefore, the conduction voltage of zero-vector freewheeling path is reduced a lot and ranged from a few hundreds milli-volts up to about 2 V with the rated power, especially, full MOSFETs are replaced with CoolMosfet.

Estimation of power device losses is critical for predicting the maximum efficiency of power electronic circuits. This section will calculate the power device losses of the Heric, H6, HB-ZVR, and two kinds of FB-CCV based on the unified circuit parameters (given in Table III), the calculation process of the device losses is consistent with [30], and interested readers are referred to reference [30]. Table I shows the device type and distribution of the device's number in the Heric, H6, HB-ZVR,

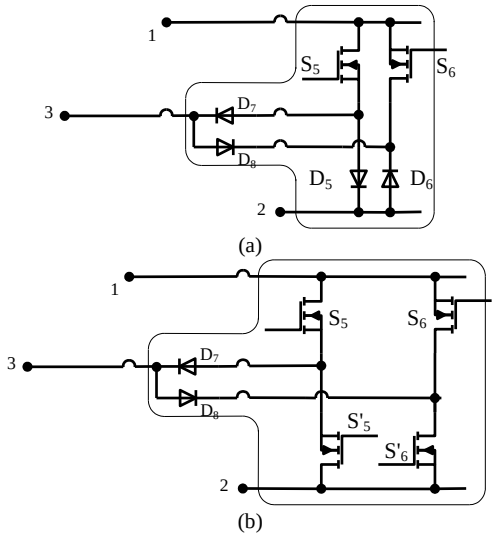

Fig. 6. Two kinds of zero-vector freewheeling paths for FB-CCV. (a) Type I: MOSFET + diode type. (b) Type II: Full MOSFETs.

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and FB-CCV, and their topologies can refer to Fig. 1(c), 1(b), 1(a), and Fig.3 (a), respectively. The IGBT and Diode are evaluated by Infineon's IKW75N60T and Advanced Power Technology's APT60DQ60B, respectively. Specially, the MOSFET of the FB-CCV-I and HB-ZVR can select Infineon's IPW65R019C7 with lower on-state resistance, the CoolMosfet of the FB-CCV-II can select Infineon's SPW47N60C3 with 7 mΩ on-state resistance, and the MOSFET of the Heric and H6 need select Infineon's IPW65R041CFD with ultra-fast body diode to freewheel the reactive power. Noteworthy, the voltage stress of the dc decoupling devices of H6 is a half the dc link voltage, for this reason 300V MOSFETs could be used theoretically. But, for safety, the devices with higher breakdown voltage ratings must be used to block whole dc link voltage in practice. The total device losses at different switching frequencies with rated power are calculated under selected device's datasheets, and are shown as histogram in Fig. 7 with each component's percent. It can be seen that the Heric is with the least device loss in the higher switching frequency span and the FB-CCV-II is with the least device loss in the lower switching frequency; The H6 and HB-ZVR have the highest device losses in low switching frequency range, and in high switching frequency range, respectively. Compared with the Heric, the FB-CCV proposed in this paper increases the turn on and off losses of the main power switches and the reverse recovery losses of the antiparallel diodes of the diagonal main power switches, and reduces the freewheeling losses; compared with the H6, the FB-CCV reduces the conduction losses significantly; compared with the HB-ZVR, the FB-CCV reduces the freewheeling losses. In particular, along with the switching frequency reducing, the device losses of the FB-CCV become closer or lower to the Heric. The calculation results are in agreement with the theoretical estimation.

TABLE I

ANALYSIS OF DEVICE OPERATION IN SEVERAL TOPOLOGIES

	Device type	Heric	H6	HB-ZVR	FB-CCV
Number	MOSFET	4	2	1	2
	IGBT	2	4	4	4
	Diode	0	2	2	4
Turn on/off loss	MOSFET	2	2	1	1
	IGBT	0	0	2	2
Conduction loss	MOSFET	2	2	0	0
	IGBT	0	2	2	2
Freewheeling loss	MOSFET	0	0	1	1
	IGBT	1	1	0	0
	Diode	1	1	2	1
Reverse recovery loss	Diode	1	1	2	2
Gate loss	MOSFET	2	2	1	2
	IGBT	0	0	2	2

B. Common-mode characteristics

A rule is concluded in literature [21], that the leakage current of a full-bridge transformerless inverter depends on the amplitude and frequency of the common-mode voltage under the condition of filter inductor symmetric placement in phase line and neutral line. According to the definition of the common-mode voltage, the common-mode voltage u_{CM} is related to u_{1N} and u_{2N}, as shown in the following:

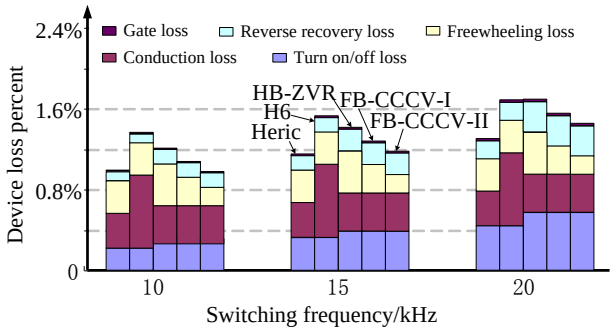

Fig. 7. Total device losses distribution for a 5-kW rate.

$$u_{CM} = \frac{u_{1N} + u_{2N}}{2} \tag{14}$$

According to the switching states and the direction of the grid-in current, the common-mode voltage can also be listed in Table II. It can be seen that the common-mode voltage is a constant value in all stages, and the FB-CCV has the best performance about leakage current suppression, likes H6 topology [30]. Therefore, the common-mode performance of the FB-CCV is better than the Heric and HB-ZVR topologies.

TABLE II

SWITCH STATES, OPERATION LEVELS, DIFFERENTIAL-MODE, AND COMMON-MODE VOLTAGE UNDER QSPWM

S_1 S_4	D_1 D_4	S_2 S_3	D_2 D_3	S_5 D_5	S_6 D_6	u_{1N}	u_{2N}	u_{DM}	u_{CM}
1	0	0	0	0	0	U_{pv}	0	U_{pv}	$U_{pv}/2$
0	0	0	1	0	0	0	U_{pv}	$-U_{pv}$	$U_{pv}/2$
0	0	0	0	0	1	$U_{pv}/2$	$U_{pv}/2$	0	$U_{pv}/2$
0	0	1	0	0	0	0	U_{pv}	$-U_{pv}$	$U_{pv}/2$
0	1	0	0	0	0	U_{pv}	0	U_{pv}	$U_{pv}/2$
0	0	0	0	1	0	$U_{pv}/2$	$U_{pv}/2$	0	$U_{pv}/2$

Note：Switching state "1" represents power device is on, and switching state "0" represents power device is off.

TABLE III

PARAMETERS OF THE PROTOTYPE

Parameter	Value
Input voltage/V	400
Grid voltage/V，frequency/Hz	220/50
Rated power/W	5000
Switching frequency/kHz	20
DC-bus capacitor C_{dc1}, C_{dc2}/μF	470μF/350V
IGBT	IKW75N60T
MOSFET for FB-CCV and HB-ZVR	IPW65R019C7
CoolMosfet for FB-CCV	SPW47N60C3
MOSFET for Heric and H6	IPW65R041CFD
Diode for freewheeling	APT60DQ60B
Diode for clamping	IDP08E65D1
Filter inductor L_1, L_2/ mH	0.5
Filter capacitor/μF	2
Common-mode inductor L_{CM}	2×B82726-S6223-N4 0 L: 2×1.6mH Turns: 11+11
Common-mode capacitor C_{Y1}、C_{Y2}/nF	22
PV parasitic capacitor C_{PV1}、C_{PV2}/μF	0.1

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IV. Experimental Results and Discussions

In order to verify and compare the operation principle and performance of the FB-CCV, HB-ZVR, Heric, and H6 topologies, a universal prototype inverter has been built in our laboratory. The specifications of the prototype are listed in Table III. The photograph of the test-bed hardware prototype is shown in Fig. 8. The procedure of testing the differential-mode and common-mode performance is consistent with reference [30].

A. Validation of the Differential-mode Characteristics

The experimental waveforms of the gate driving signals of the FB-CCV are shown in Fig. 9. It can be seen that a dead time is added in the current zero-crossing period, which is in agreement with Fig. 3(c). Fig. 10 (a), (b) and (c) show the experimental waveforms of the grid voltage u_g, the grid-in current i_g, and the differential-mode voltage u_{DM} at the grid frequency scale, in the FB-CCV or HB-ZVT with qSPWM, Heric or H6 with unipolar SPWM, and conventional full-bridge H4 topology with bipolar SPWM, respectively. Obviously, the differential-mode voltage of the FB-CCV and HB-ZVT is different with the unipolar SPWM and bipolar SPWM modulation. Fig. 11 (a) and (b) show the experimental waveforms of the FB-CCV including the driving signals of S_1 and S_5, the inductor current i_L, and the differential-mode voltage u_{DM} at switching frequency scale, in the positive half period and the negative half period of the grid-in current, respectively. It can be seen that the dead time between the complementary switches S_1 and S_5 is about 2μs, and the differential-mode voltage of the FB-CCV has three levels in each switching period, which is agreement with the theoretical analysis. Referring to the waveforms of the filter inductor

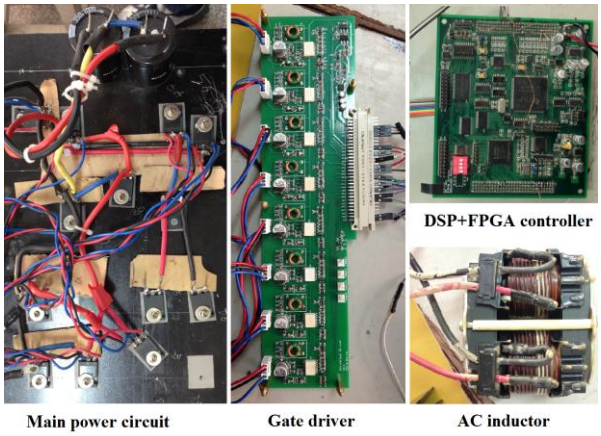

Fig. 8. Test-bed hardware prototype.

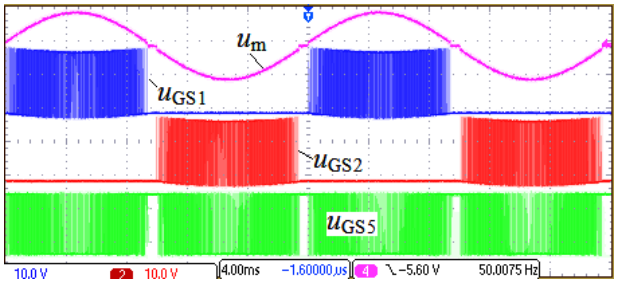

Fig. 9 Experimental waveforms of the modulation and driving signals. (u_m: 5V/div, u_{GS1}, u_{GS2}, and u_{GS5}: 10V/div, and time: 4ms/div)

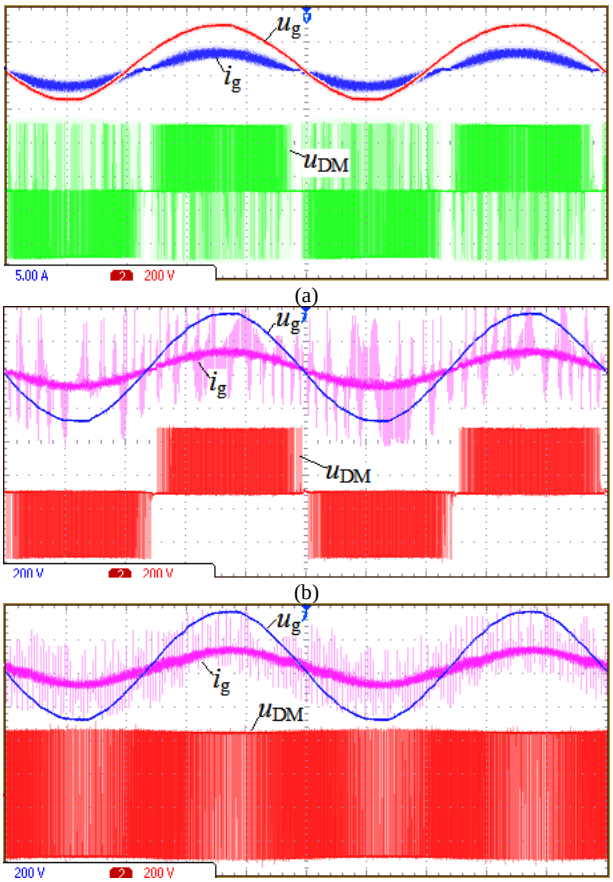

Fig. 10. Experimental waveforms of the grid voltage, the grid-in current, and the differential-mode voltage at the grid frequency scale. (a) FB-CCV or HB-ZVR with qSPWM. (b) Heric or H6 with unipolar SPWM. (c) H4 with bipolar SPWM. (u_g and u_{DM}: 200V/div, i_g: 5A/div, and time: 4ms/div)

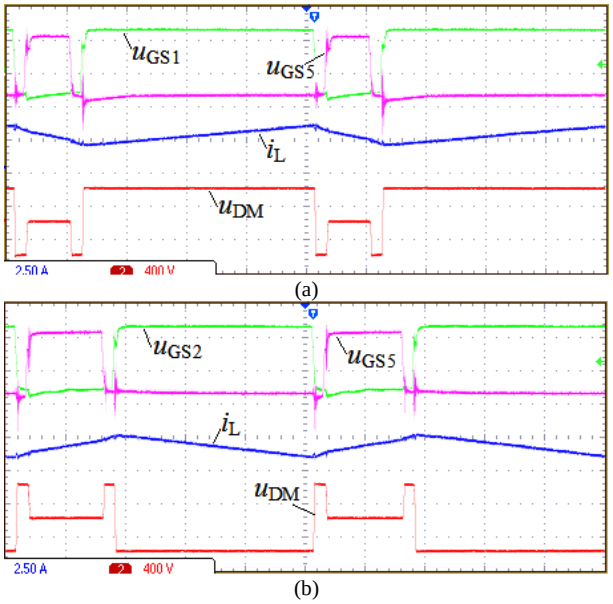

Fig. 11. Experimental waveforms of the driving voltage, the inductor current, and the differential-mode voltage at the switching frequency scale. (a) In positive half period. (b) In negative half period. (u_{GS1}, u_{GS2}, and u_{GS5}: 10V/div, i_L: 2.5A/div, u_{DM}: 400V/div, and time: 4μs/div)

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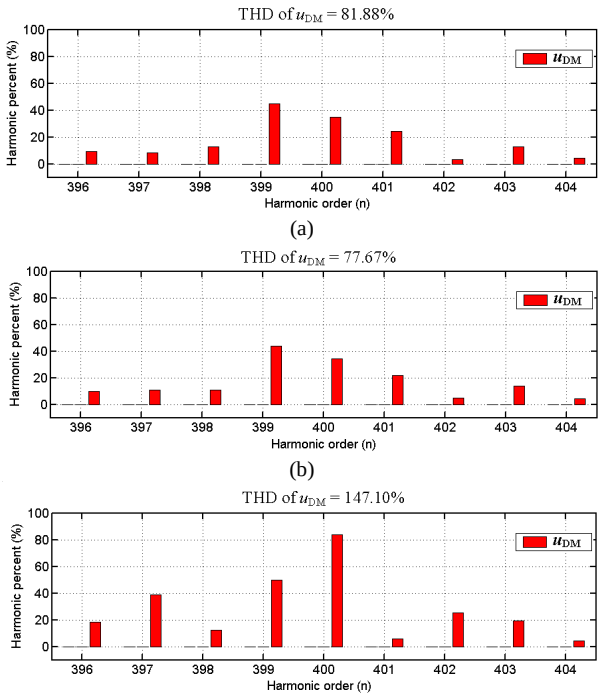

Fig. 12. Harmonic spectrum of the inductor current, and the differential-mode voltage in the switching frequency vicinity. (a) FB-CCV or HB-ZVR with qSPWM. (b) Heric or H6 with unipolar SPWM. (c) H4 with bipolar SPWM.

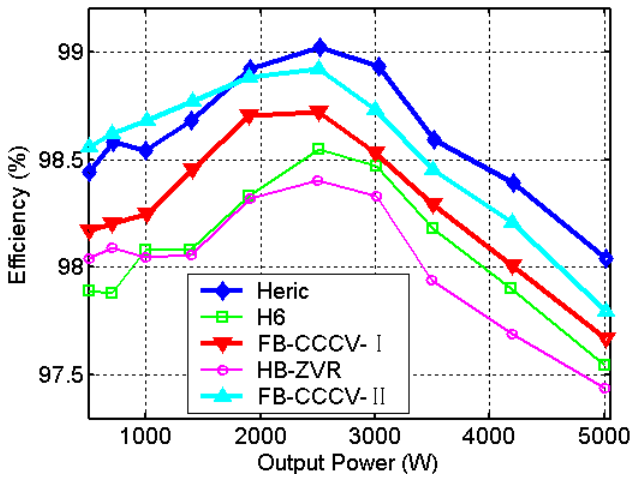

Fig. 13. Measured efficiency as a function of the output power with switching frequency at 20kHz.

current in Fig. 11, it can be seen that the part of the bipolar modulation has only a little influence on inductor current during the dead time, and the ripple of the filter inductor current is closest to the unipolar SPWM modulation which has lower filter losses.

Fig. 12 (a), (b) and (c) show the harmonic spectrum of the differential-mode voltage u_{DM} in switching frequency vicinity, and the total THD in the FB-CCV or HB-ZVR with qSPWM, the Heric or H6 with unipolar SPWM, and the conventional full-bridge H4 topology with bipolar SPWM, respectively. It can be seen that the THD of the harmonic spectrum with the qSPWM is very close to the unipolar SPWM, and far lower than the bipolar SPWM, and the experimental data are in agreement with the theoretical analysis and the waveforms estimation.

Fig. 13 shows, for the Heric, H6, HB-ZVR, FB-CCV-I and FB-CCV-II, their efficiencies as a function of the output power, which has been measured by Digital Power Analyzer PM3300 from VOLTECH. Note that the presented efficiency diagram covers the losses of the main power stage including power semiconductor device losses and output inductor losses, but it does not include the power consumption of control circuit and the associated driver circuit. The measured data are in agreement with the trend of theoretical calculation in Fig. 7.

B. Validation of the Common-mode Characteristics

Fig. 14 (a), (b), (c) and (d) show the experimental waveforms of the grid voltage u_g, the grid-in current i_g, the voltage u_{1N}

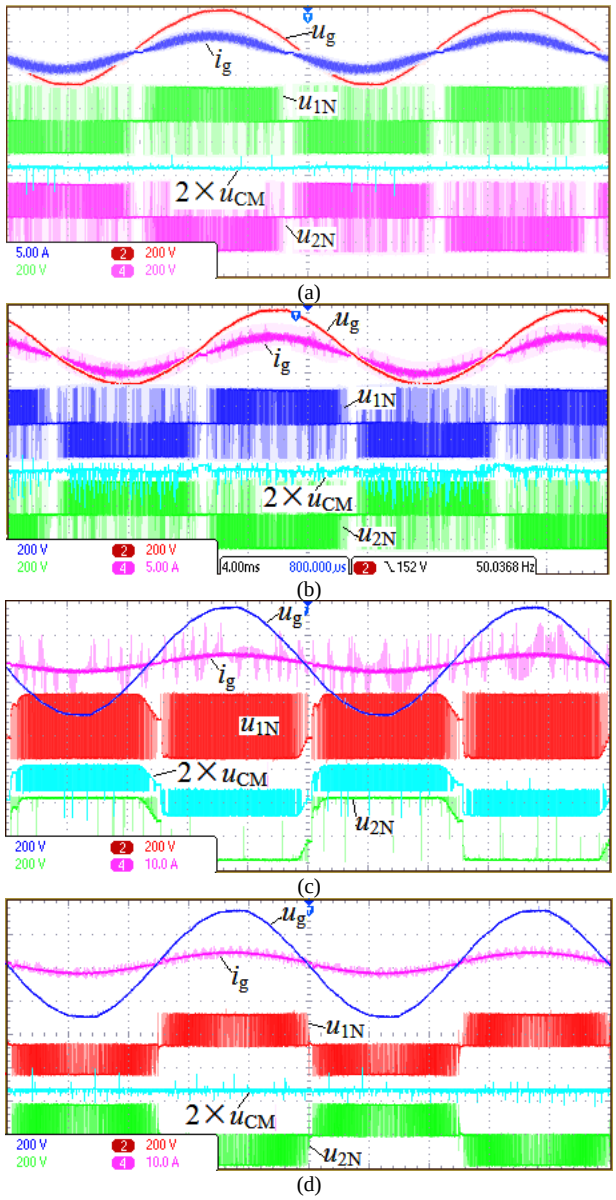

Fig. 14. Experimental waveforms of the grid voltage, the grid-in current, and the common-mode voltage at the grid frequency scale (u_g, u_{1N}, u_{2N}, and u_{CM}: 200V/div, i_g: 5A/div, and time: 4ms/div). (a) FB-CCV; (b) HB-ZVR; (c) Heric (i_g: 10A/div); (d) H6 (i_g: 10A/div)

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between the midpoints 1 and N, the voltage u_{2N} between the midpoints 2 and N and the common-mode voltage u_{CM} at the grid frequency scale, in the FB-CCV, HB-ZVR, Heric, and H6, respectively. Obviously, the common-mode voltage of the FB-CCV is a constant value including the current zero-crossing period, likes H6. Fig. 15(a) and (b) show the experimental waveforms of the grid voltage u_g, the inductor current i_L, the voltage u_{1N}, the voltage u_{2N}, and the common-mode voltage u_{CM} at switching frequency scale, respectively. It can be seen that in the zero-vector freewheeling period, the common-mode voltage is effectively clamped by the passive diodes. Table IV lists the experimental data of the leakage current under the unified circuit parameters with 1kW output power, in the Heric, H6, HB-ZVR, and FB-CCV, respectively, the test step and the measuring method can refer to [30]. From the Table IV, the common-mode characteristic of the FB-CCV is similar with the H6 topology. The experimental results are in agreement with the theoretical analysis well.

Fig. 16 shows the midpoint voltage u_{3N} of the capacitor divider of the FB-CCV, the input voltage u_{PV}, and the current i_D of the clamping branch, respectively. It is obvious that the capacitor voltage is divided well, and the current in the clamping path is very small. The reason is that the imbalance voltage is limited by the impedance of the common-mode paths, this impedance is far more than the differential-mode path's. Therefore, the rated current of the diodes D7 and D8 are little. To guarantee that the capacitor divider of the FB-CCV works well, a simplified and reliable voltage-balancing circuit is adopted also in the prototype, its operation principle can refer to [33].

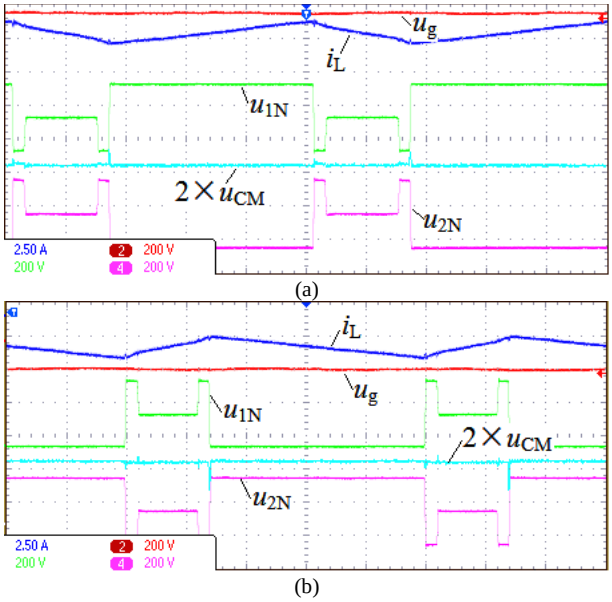

Fig. 15. Experimental waveforms of the grid voltage, the grid-in current, and the common-mode voltage at the switching frequency scale. (a) In positive half period; (b) In negative half period. (u_g, u_{1N}, u_{2N}, and u_{CM}: 200V/div, i_L: 2.5A/div, and time: 4μs/div)

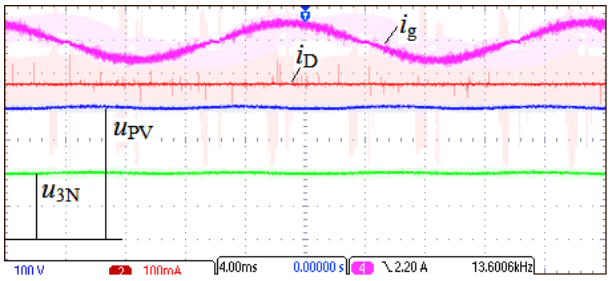

Fig. 16. Experimental waveforms of the capacitor divider, and the clamping current. (u_{PV} and u_{3N}: 100V/div, i_D: 100mA/div, i_g: 5A/div, and time: 4ms/div)

TABLE IV
EXPERIMENTAL DATA OF LEAKAGE CURRENT AT SWITCHING FREQUENCY

Topology	Value
Heric	5.6 mA
H6	0.7 mA
HB-ZVR	2.1mA
FB-CCV	0.6mA

V. CONCLUSION

A quasi-unipolar SPWM full-bridge inverter topology with two unidirectional freewheeling braches and a passive clamping branch has been proposed in this paper. The proposed inverter has the following characteristics: (i) The quasi-unipolar SPWM differential-mode voltage is a combination of unipolar and bipolar SPWM, and is more close to the unipolar SPWM. (ii) There are two operation modes in the freewheeling period: the dead-time freewheeling mode and zero-vector freewheeling mode, which guarantee that the high-frequency common-mode voltage is on a constant value in whole switching period. (iii) The freewheeling paths have two kinds of combinations: MOSFET + diode, or full MOSFETs, meanwhile, the full MOSFETs type freewheeling path can reduce the conduction loss further. The proposed inverter is an optimized topology with high conversion efficiency and low leakage current.

These merits are verified and compared by a universal prototype. It can be concluded that the proposed topology is extremely suitable for transformerless single-phase grid-connected inverter with lower switching frequency.

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