Hybrid Transformer ZVS/ZCS DC–DC Converter With Optimized Magnetics and Improved Power Devices Utilization for Photovoltaic Module Applications

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***Abstract*—This paper presents a nonisolated, high boost ratio dc–dc converter with the application for photovoltaic (PV) modules. The proposed converter utilizes a hybrid transformer to incorporate the resonant operation mode into a traditional high boost ratio active-clamp coupled-inductor pulse-width-modulation dc–dc converter, achieving zero-voltage-switching (ZVS) turn-on of active switches and zero-current-switching turn-off of diodes. As a result of the inductive and capacitive energy being transferred simultaneously within the whole switching period, power device utilization (PDU) is improved and magnetic utilization (MU) is optimized. The improved PDU allows reduction of the silicon area required to realize the power devices of the converter. The optimized MU reduces the dc-bias of magnetizing current in the magnetic core, leading to smaller sized magnetics. Since the magnetizing current has low dc-bias, the ripple magnetizing current can be utilized to assist ZVS of main switch, while maintaining low root-mean-square (RMS) conduction loss. The voltage stresses on the active switches and diodes are maintained at a low level and are independent of the wide changing PV voltages as a result of the resonant capacitor in series in the energy transfer loop. The experimental results based on 250 W prototype circuit show 97.7% peak efficiency and system CEC efficiencies greater than 96.7% over 20 to 45 V input voltages. Due to the high efficiency over wide power range, the ability to operate with a wide variable input voltage and compact size, the proposed converter is an attractive design for PV module applications.**

***Index Terms*—High CEC efficiency, hybrid transformer, improved power device utilization (PDU), low device voltage stresses, optimized magnetic utilization (MU), PV modules.**

I. Introduction

GLOBAL demand for electrical energy is constantly increasing. Due to the declining production and the rising cost of nonrenewable energy supplies, there has been a growing demand for the utilization of renewable energy sources. Among these renewable energy sources, photovoltaic (PV) energy has experienced remarkable growth over the past decades.

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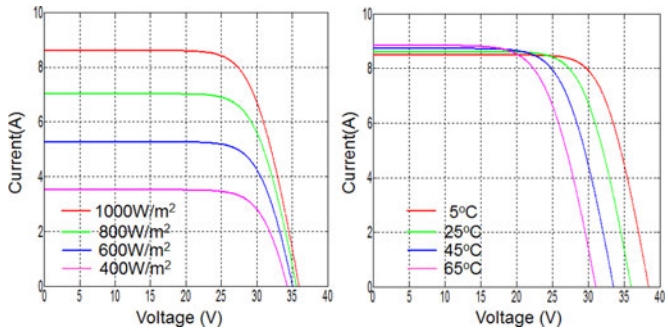

Fig. 1. *I–V* curves of CS6P-240P PV module from Canadian Solar Inc.

The PV energy generated from sunlight is captured by dc PV modules. The power generated by these modules is integrated into the existing ac power distribution infrastructure through the power conditioners [1]–[3], which can adopt two-stage or single-stage system configurations. Compared to single-stage systems, the two-stage single-phase architecture can use the high-voltage dc-bus as double-line ripple power buffer to avoid failure-prone electrolyte capacitors [4]–[6]. In two-stage PV power conditioners, high boost ratio dc–dc converters are used to increase the low PV voltage to a high dc voltage to interface the PV modules with either a low-power individual inverter or a high power centralized grid-connected inverter [1]–[3]. Since galvanic insulation is not mandatory in code, this high boost ratio dc–dc converter can be isolated or nonisolated [1], [4]–[8].

Fig. 1 shows a cluster of *I–V* curves based on datasheet of a 240-W PV module CS6P-240P from CanadianSolar [9] at different irradiance levels and environmental temperatures. Due to the different output voltage and power from the PV panel, it would be beneficial to have a high boost ratio dc–dc converter with a high efficiency over the entire PV voltage and output power ranges to maximize energy yield during different operating conditions. Another requirement for this high boost ratio dc–dc converter is to have high power density and low profile to integrate with the PV modules. With the PV module costs continuously dropping, the electrics cost is becoming increasingly dominant. This requires that the dc–dc converter to have simple structure and low electronic cost.

Of the high boost ratio dc–dc converter topologies presented [6], [8]–[27], the uses of coupled-inductor are attractive due to the fact that only one magnetics is required and low voltage active switches can be utilized. The reason that the primary

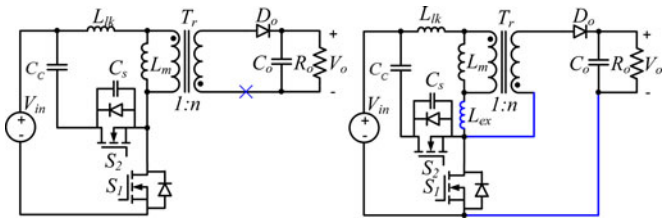

Fig. 2. (a) Active-clamp flyback converter. (b) Active-clamp coupled-inductor high boost ratio converter.

side active switches of the high boost ratio converters have low voltage stress comes from the transformer effect of the coupled-inductors. Since the primary active switches have low voltage stresses, the circuits can use low voltage MOSFETs that generally have a low $R_{\mathrm{ds(on)}}$ and fast switching speed, decreasing both the conduction and switching losses. To further reduce the switching losses, active-clamp techniques have been widely used [19], [24], [27]–[29], A zero-voltage-switching (ZVS) high boost ratio active-clamp coupled-inductor (ACCI) converter, as shown in Fig. 2(b), was presented in [19]. This converter could be derived from traditional active-clamp flyback converter [28], [29], as shown in Fig. 2(a), by splitting secondary side and series connecting the output winding with the clamping capacitor C_c. Besides inheriting the simple structure, low voltage stresses and ZVS operation of active switches, the boost ratio of this converter was increased. This allows designing coupled-inductor with lower turns ratio, which reduces the primary-side root-mean-square (RMS) conduction losses. As a result of increased boost ratio, the voltage stresses of the active switches were reduced, allowing use of low-voltage MOSFET switches with low $R_{\mathrm{ds(on)}}$. However, voltage stress on the output diode of ACCI converter is still high as that of traditional active-clamp flyback converter. To reduce voltage ringing across the output diode, a passive snubber was added [19], which degraded the efficiency of the converter. Similar to traditional active-clamp flyback converter, the ACCI converter only transfers energy to the secondary side during the interval when the main switch is off, causing poor magnetic utilization (MU) and high dc-bias magnetizing current. In order to avoid high ripple current, the energy stored in the leakage and/or external inductors instead of energy in magnetizing inductance [19], [28]–[29] has been utilized to achieve ZVS of main switch. However, a large leakage or external inductance results in a loss of effective duty cycle on the secondary side of coupled-inductor. Normally, a transformer with higher turns ratio is required to compensate the secondary-side duty loss. With a higher turns ratio, the reflected output current into the primary side is increased, which results in higher primary-side conduction losses. Besides, the higher turns ratio increases the voltage stress of the output diode. The conflict between low conduction losses and low switching losses prevented this converter to achieve high efficiency over wide power range. This is not desirable for PV module power conversion where the high efficiency over a wide power is required because the performance is weighted differently for specific power levels in the California Energy Commission (CEC) or European Union (EU) standards.

In this paper, a high boost ratio ZVS/ZCS dc–dc converter with hybrid transformer [6], [30] is presented to achieve high

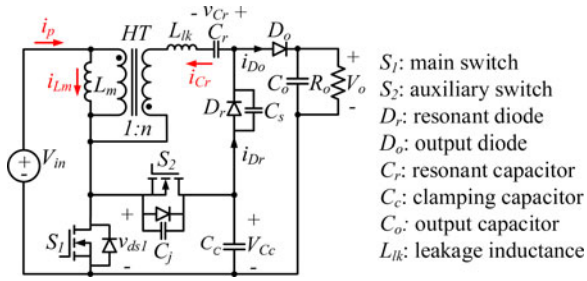

Fig. 3. Proposed high boost ratio ZVS/ZCS dc–dc converter with hybrid transformer.

system level efficiency over wide input voltage and power ranges. By adding a small resonant capacitor and a resonant diode into the previous ACCI converter [19], a hybrid operation mode [6], [30] which combines pulse-width-modulation (PWM) and resonant power conversions, is introduced into the proposed high boost ratio converter. This converter utilizes a hybrid transformer that combines the modes where the transformer operates under normal conditions and where it operates as a coupled-inductor to transfer the energy to high voltage side improving the utilization of the magnetic core. The dc-bias of the magnetizing current can be effectively reduced and smaller sized magnetics can be utilized. Due to the low dc-bias of the magnetizing current the proposed converter can be designed with small magnetizing inductance allowing bidirectional magnetizing current flow to achieve ZVS of main switch while maintaining low RMS conduction loss. The output diodes in the proposed converter can achieve zero-current-switching (ZCS) turn-off because the resonant currents resonate back to zero at the switching transitions. The continuous input current with combined sinusoidal resonant and linear PWM current leads to smaller current ripple and reduced RMS conduction losses. The voltage stresses on the active switches and diodes are maintained at a low level and are independent of the wide changing input PV voltages as a result of the resonant capacitor in series in the energy transfer loop. Due to reduced switching losses achieved by ZVS and ZCS operations and reduced RMS conduction losses, the proposed converter can achieve high system efficiency over wide input voltage and power ranges. The performance of the proposed converter was verified experimentally utilizing a 250-W prototype circuit with the PV module voltages from 20 to 45 V. Experimental results indicate that the specific input voltage ranges within which the proposed converter has highest CEC efficiencies match the maximum power point ranges of *I–V* curves of PV module datasheet, which ensures maximum energy yield from the PV modules.

II. Proposed Converter Topology and Operation Analysis

Fig. 3 shows the circuit diagram of the proposed converter. *HT* is a hybrid transformer with primary to secondary turns ratio 1:*n* and with secondary-reflected equivalent leakage inductance L_{lk}; S_1 is the main switch and S_2 is the auxiliary active-clamp switch; C_c is the clamping capacitor; D_r is a resonant diode, which provides a unidirectional current flow path to charge the resonant capacitor C_r when S_1 is on; D_o is the output diode;

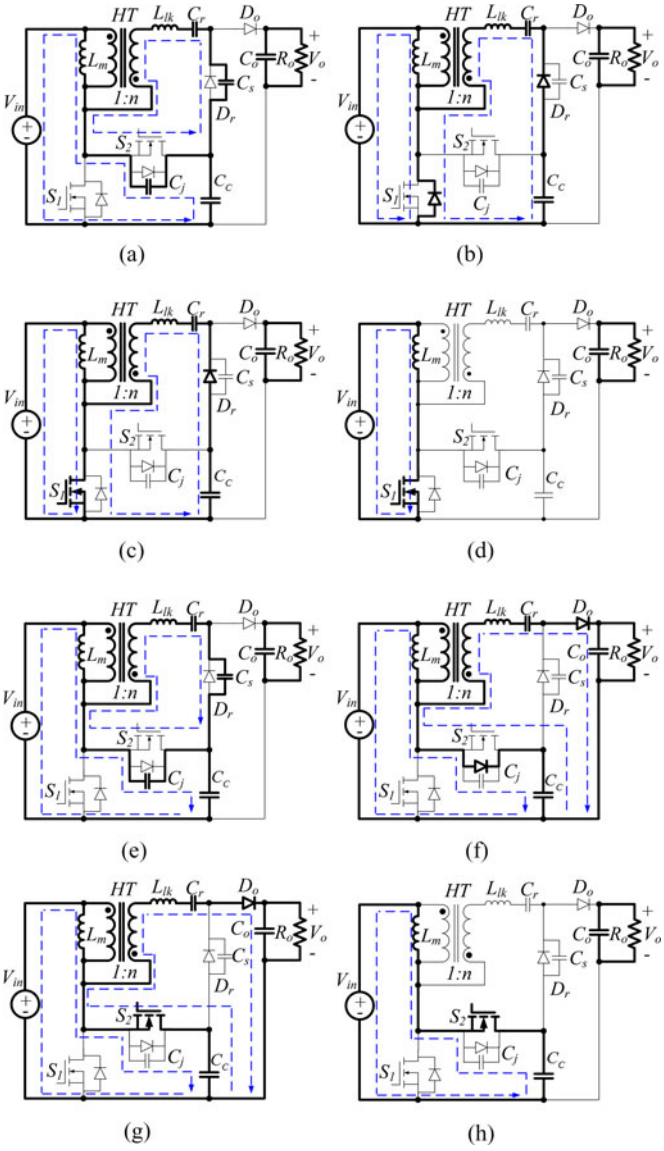

Fig. 4. Topological stages: (a) t0-t1, (b) t1-t2, (c) t2-t3, (d) t3-t4, (e) t4-t5, (f) t5-t6, (g) t6-t7, and (h) t7-t8.

C_j represents the equivalent parasitic junction capacitors of MOSFETs, C_s is the equivalent capacitor of the diodes D_o and D_r, C_o is the output capacitor; R_o is the equivalent resistive load, and $V_{\rm in}$ represents PV-side equivalent voltage.

Fig. 4 illustrates the eight steady-state topological states of the proposed converter within one switching cycle. Fig. 5 shows the key voltage and current waveforms for specific devices over one switching cycle. In Fig. 5, g_1 and g_2 represent the driver signals to S_1 and S_2 and the definition of other notations is represented in Fig. 3. For the description of the circuit operation and for the subsequent design procedure in the followed sections, the following assumptions are made:

1) ideal MOSFET switches S_1 and S_2 with body diodes;
2) D is the steady-state duty ratio based on S_1;
3) the voltage ripples on C_o and C_c are negligibly small.

The sequence of topological states is described as below.

t_0–t_1: At t_0, S_2 is turned off. The negative magnetizing current i_{L_m} starts to charge C_j. Due to the voltage potential change

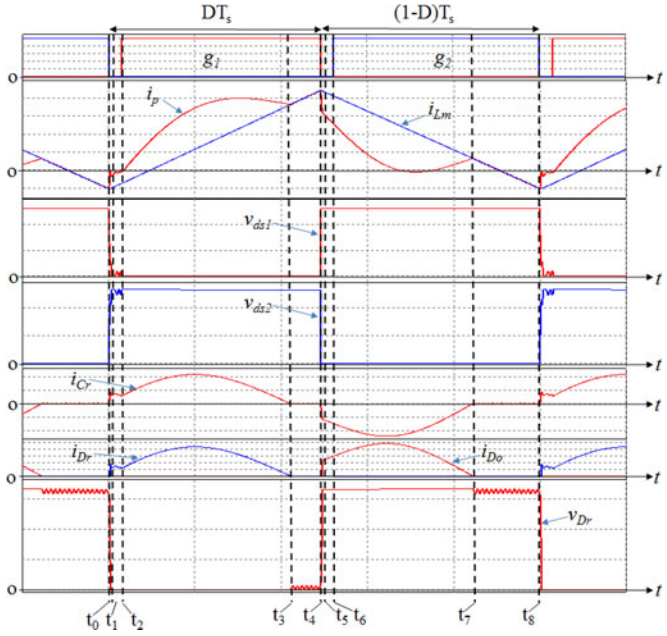

Fig. 5. Steady-state waveforms.

of the drain node of S_1, a parasitic minor resonant loop composed of secondary side of *HT*, L_{lk}, C_r, C_s, and C_j starts to resonate until D_r is forward-biased.

t_1–t_2: At t_1, $v_{\rm ds1}$ is reduced to zero. i_{s1}, which is equal to the sum of i_p and ni_{Cr}, flows through the body diode of S_1. This provides a ZVS condition for S_1. $V_{\rm in}$ is applied on L_m and i_{L_m} is linearly increased. Meanwhile, the secondary-reflected input voltage $nV_{\rm in}$ along with V_{Cc} charge C_r in a resonant manner through the resonant loop including secondary side of *HT*, L_{lk}, C_r, D_r, C_c and body diode of S_1.

t_2–t_3: At t_2, S_1 is turned on with ZVS. The state equations of secondary resonant circuit from t_1 to t_3 can be written as follows:

$$L_{lk}\frac{{\rm d}i_{Cr}}{{\rm d}t} = nV_{\rm in} + V_{Cc} - v_{Cr} \tag{1}$$

$$C_r\frac{{\rm d}v_{Cr}}{{\rm d}t} = i_{Cr} \tag{2}$$

From (1) and (2), i_{Cr} and v_{Cr} can be calculated as

$$i_{Cr}(t) = \frac{nV_{\rm in} + V_{Cc} - v_{Cr}(t_1)}{Z_{r1}}\sin\omega_{r1}(t-t_1) \tag{3}$$

$$v_{Cr}(t) = nV_{\rm in} + V_{Cc} - (nV_{\rm in} + V_{Cc} - v_{Cr}(t_1))\cos\omega_{r1}(t-t_1) \tag{4}$$

where Z_{r1} and ω_{r1} are the angular resonant frequency and impedance given by $Z_{r1} = \sqrt{L_{lk}/C_{\rm eq1}}, \omega_{r1} = \sqrt{1/L_{lk}C_{\rm eq1}}$, $C_{\rm eq1} = \frac{C_rC_c}{(C_r+C_c)} \approx C_r (C_c \gg C_r)$.

t_3–t_4: At t_3, $i_{\rm Dr}$ resonates back to zero so D_r turns off with ZCS. $V_{\rm in}$ continues to linearly charge L_m. From t_1 to t_4, i_{L_m} is linearly charged by $V_{\rm in}$ and is given by

$$i_{L_m}(t) = i_{L_m}(t_1) + \frac{V_{\rm in}}{L_m}(t-t_1) \tag{5}$$

t_4–t_5: At t_4, S_1 is turned off. i_{L_m} starts to discharge C_j. Due to the voltage potential change of the drain node of S_1, a parasitic minor resonant loop composed of secondary side of *HT*, L_{lk}, C_r, C_s, and C_j starts to resonate.

t_5–t_6: At t_5, C_s is discharged to the point where the antiparallel diode of S_2 starts to conduct. This provides ZVS turn-on of S_2. Also, the voltage potential of anode of D_o increases high enough leading D_o to be forward-biased.

t_6–t_7: At t_6, S_2 is turned on with ZVS. Since it takes a long time interval before i_{L_m} reduces to zero, ZVS of S_2 is easily achieved. The energy is transferred to the output with the resonant current i_{D_o}. The state equations of secondary resonant circuit from t_5 to t_7 can be written as follows:

$$L_{lk}\frac{\mathrm{d}i_{Cr}}{\mathrm{d}t} = n(V_{\mathrm{in}} - V_{Cc}) + V_o - V_{Cc} - v_{Cr} \tag{6}$$

$$C_r\frac{\mathrm{d}v_{Cr}}{\mathrm{d}t} = i_{Cr} \tag{7}$$

From (6) and (7), i_{Cr} and v_{Cr} can be calculated as

$$i_{Cr}(t) = \frac{nV_{\mathrm{in}} - (n+1)V_{Cc} + V_o - v_{Cr}(t_7)}{Z_{r2}}\sin\omega_{r2}(t-t_5) \tag{8}$$

$$v_{Cr}(t) = nV_{\mathrm{in}} - (n+1)V_{Cc} + V_o - (nV_{\mathrm{in}} - (n+1)V_{Cc} + V_o - v_{Cr}(t_7))\cos\omega_{r2}(t-t_5) \tag{9}$$

where $Z_{r2} = \sqrt{L_{lk}/C_{\mathrm{eq2}}}, \omega_{r2} = \sqrt{1/L_{lk}C_{\mathrm{eq2}}}$. C_{eq2} is the equivalent capacitance with C_c, C_o, C_r and C_c/n^2 in series. However for a well-designed converter, the capacitance of C_c and C_o is normally much higher than C_r, so we have $C_{\mathrm{eq2}} \approx C_r$.

t_7–t_8: At t_8, i_{D_o} resonates to zero, D_o turns off with ZCS. From t_5 to t_8, the voltage applied on L_m is V_{in}–V_{Cc}, which decreases i_{L_m} to a negative valley to provide a ZVS turn-on condition of S_1. i_{L_m} *within* t_5–t_8 can be calculated by

$$i_{L_m}(t) = i_{L_m}(t_5) + \frac{V_{\mathrm{in}} - V_{Cc}}{L_m}(t-t_5) \tag{10}$$

Assuming the switching transition periods of t_0–t_1 and t_4–t_5 are negligibly short, the boost ratio M_b can be derived by three flux balance criteria in the steady state. The first flux balance equation which governs the circuit is from the flux balance of L_m during the whole switching period. This can be obtained from (5) and (10) as

$$\int_0^{T_s} L_m i_{L_m}(t)\mathrm{d}t = \int_{t_1}^{t_4} V_{\mathrm{in}}\mathrm{d}t + \int_{t_5}^{t_8}(V_{\mathrm{in}} - V_{Cc})\mathrm{d}t = \int_0^{DT_s} V_{\mathrm{in}}\mathrm{d}t + \int_{DT_s}^{T_s}(V_{\mathrm{in}} - V_{Cc})\mathrm{d}t = 0 \tag{11}$$

Second flux balance equation can be derived from (3) according to flux balance on L_{lk} within the period t_1–t_3

$$\int_{t_1}^{t_3} L_{lk} i_{Cr}(t)\mathrm{d}t = \int_{t_1}^{t_3} L_{lk}\frac{nV_{\mathrm{in}} + V_{Cc} - v_{Cr}(t_1)}{Z_{r1}}\sin\omega_{r1}(t-t_1)\mathrm{d}t = 0 \tag{12}$$

TABLE I
SPECIFICATION AND POWER STAGE PARAMETERS

Converter	ACCI converter	Proposed converter
Rated power	250 W	250 W
Output voltage	380 V	380 V
Input voltage range	20–45 V	20–45 V
Output power range	25W∼250 W	25W∼250 W
Turns ratio	$n_1 = 70/3$	$n_2 = 16/3$
Switching frequency	100 kHz	100 kHz
Magnetizing inductor	$L_{m1} = 20\ \mu$H	$L_{m2} = 5.6\ \mu$H
Clamping capacitor	$C_c = 20\ \mu$F	$C_c = 20\ \mu$F
External inductor	$L_{\mathrm{ex}} = 1\ \mu$H	N.A.
Resonant capacitor	NA	$C_r = 0.40\ \mu$F
R-C snubber	Yes	N.A.

Similarly, the last flux balance can be derived from (8) according to flux balance on L_{lk} within the period t_5–t_7

$$\int_{t_5}^{t_7} L_{lk} i_{Cr}(t)\mathrm{d}t = \int_{t_5}^{t_7} L_{lk}\frac{nV_{\mathrm{in}} - (n+1)V_{Cc} + V_o - v_{Cr}(t_5)}{Z_{r2}} \times \sin\omega_{r2}(t-t_5)\mathrm{d}t = 0 \tag{13}$$

Normally, the ripple voltage on C_r is small compared to the average voltage V_{Cr} of C_r. Replacing V_{Cr} into (12) and (13) and solving (11), (12) and (13) yields

$$M_b = \frac{V_o}{V_{\mathrm{in}}} = \frac{n+2}{1-D} \tag{14}$$

$$V_{Cr} = \frac{n+1-D\cdot n}{n+2}V_o \tag{15}$$

$$V_{Cc} = \frac{V_{\mathrm{in}}}{1-D} = \frac{V_o}{n+2} \tag{16}$$

Equation (14) reveals that the conversion ratio of the proposed converter is similar to the conventional boost converter except for additional $n+1$ gain boost. This boost gain feature is very beneficial to implement an inner voltage control loop inside the maximum power point tracking (MPPT) loop to reject the double-line-current from the following-stage single-phase inverter since it is like a buck converter from the output to input [4], [5].

III. ADVANTAGES AND DESIGN CONSIDERATIONS

The advantages of the proposed converter are analyzed in this section to highlight its suitability for PV module applications. The specifications of PV module used for the analysis in this section and for system experimental verification is CS6P-240P [9] from CanadianSolar. In order to demonstrate the improvements of introducing resonant operation into traditional PWM converters, the high boost ratio ACCI converter in [19] and the proposed converter will be comparatively analyzed. The specification requirements and the parameters of two prototype converters are shown in Table I.

For the following analysis, the notations with subscripts 1 and 2 represent ACCI converter in [19] and the proposed converter respectively.

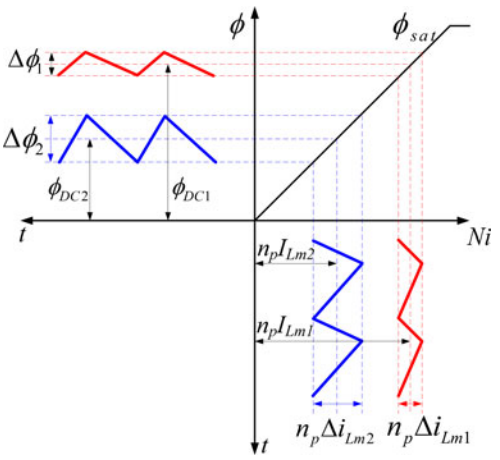

Fig. 6. Total flux in the magnetic core versus MMF: variables with subscript 1 are for converter in [19], variables with subscript 2 are for the proposed converter; n_p is primary turns.

A. Optimized Magnetic Utilization Over Conventional PWM High Boost Ratio ACCI Converter in [19]

One dominant factor of the volume of PV module integrated dc–dc converter is the magnetic component. Two methods can be employed to reduce the magnetic size, one is increasing the switching frequency, and another is optimizing the MU. However, one barrier of high switching frequency operation is the high efficiency. Hence, improving the MU is very beneficial to reduce the size of the PV module integrated dc–dc converter. The required core-window product, i.e. the size of magnetic component is proportional to the energy store in the magnetic core [31]

$$A_eW_a \propto \frac{1}{2}L_mI_mi_{m\_pk} \tag{17}$$

where, L_m is the magnetizing inductance, I_m and i_{m_pk} is the average and peak magnetizing current respectively. In the proposed converter and conventional coupled-inductor based PWM high boost ratio converters, air gap is normally required to store the magnetic energy and prevent saturation. The gapped magnetic core has linear reluctance; hence the total flux in the magnetic core versus magnetomotive force (MMF) for the proposed converter and the ACCI converter in [19] can be illustrated as in Fig. 6. The dc-bias current for converter in [19] can be calculated as

$$I_{Lm1} = \frac{(D_1n_1+1)}{(1-D_1)\cdot D_1}\frac{P_o}{V_o} \tag{18}$$

The dc-bias current for proposed converter can be calculated as

$$I_{Lm2} = \frac{(n_2+2)}{(1-D_2)}\frac{P_o}{V_o} \tag{19}$$

In (18) and (19), D_1 and D_2 are the duty cycles for 30 V PV input voltage; P_o is the maximum output power 250 W; V_o is output voltage and equal to 380 V.

The ripple magnetizing currents of the converter in [19] and the proposed converter can be calculated as

$$\Delta i_{Lm1} = \frac{(1-D_1)\cdot D_1}{(D_1n_1+1)}\frac{V_o}{f_{sw}L_{m1}} \tag{20}$$

$$\Delta i_{Lm2} = \frac{(1-D_2)\cdot D_2}{n_2+2}\frac{V_o}{f_{sw}L_{m2}} \tag{21}$$

The ratio of the required core-window product of magnetic component between the proposed converter and the ACCI converter is expressed as

$$R_{A_eW_a} = \frac{\frac{1}{2}L_{m2}I_{Lm2}\cdot(I_{Lm2}+\frac{\Delta i_{Lm2}}{2})}{\frac{1}{2}L_{m1}I_{Lm1}\cdot(I_{Lm1}+\frac{\Delta i_{Lm1}}{2})} \tag{22}$$

Substituting (17) to (21) into (22), $R_{A_eW_a}$ is calculated equal to 0.467, which means that the required core-window product of magnetic component in the proposed converter is much smaller than the traditional PWM ACCI converter. In other words, the MU in the proposed converter is greatly improved. Hence, smaller sized magnetics can be used in the proposed converter for transferring same rated power, which allows low profile design to integrate with PV module.

The reason of improved MU in the proposed converter is because the magnetics works as a hybrid transformer [6], [30] that transfers the energy to high voltage side combined with the normal transformer and coupled-inductor operations. While in the traditional PWM ACCI converter, the magnetics simply worked as a coupled-inductor.

B. Low Voltage Stresses of Power Devices, Independent of Wide Changing PV Voltages

For the proposed converter, the voltage stresses on S_1 and S_2 are equal to the clamping capacitor voltage V_{Cc}, which can be obtained from (16) as

$$V_{S_1} = V_{S_2} = V_{Cc} = \frac{V_o}{n+2} \tag{23}$$

Equation (23) shows that the voltage stresses on the active switches are only dependent on the output high dc-bus voltage and the turns ratio. By optimally designing the turns ratio, the voltage stresses on the active switches maintain a low level and are independent of the wide changing PV voltage and the duty cycle. This feature allows utilization of low breakdown voltage switches with low $R_{\mathrm{ds(on)}}$ to significantly reduce the conduction loss.

The voltage stresses diodes D_r and D_o are easily obtained as

$$V_{Dr} = V_{Do} = V_o - V_{Cc} = \frac{n+1}{n+2}V_o \tag{24}$$

We can use 500 V diodes for the proposed converter. However, for conventional high boost ratio PWM converters [19], 1000 V or even higher breakdown voltage diodes with high forward voltage drop and poor switching performance are required.

C. Improved Power Device Utilization Over Conventional PWM High Boost Ratio ACCI Converter [19]

The suitability of a power electronics topology for a specific application can be evaluated by power device utilization (PDU)

[32]. The PDU can be defined as [32]

$$\text{PDU} = \frac{P_{\max}}{\sum_{j=1}^{k} V_j I_j} \tag{25}$$

where V_j is the peak voltage applied to semiconductor device j, and I_j is the RMS or peak current applied to device j. A good candidate topology for a specific application should have minimized voltages and currents imposed on the semiconductor devices, while the transferred power is maximized. Improving the device utilization leads to minimization of the silicon area required to realize the power devices of the converter. The voltage stresses across main switch S_1, auxiliary switch S_2 and output diode D_o in ACCI converter are given by

$$V_{S_1} = V_{S_2} = \frac{V_{\text{in}}}{(1 - D_1)} \tag{26}$$

$$V_{Do} = n_1 \frac{V_i L_{m1}}{(L_{m1} + L_k)} + V_o \tag{27}$$

The peak current through S_1 and S_2 are given by

$$I_{S_1,pk} = I_{S_2,pk} = \frac{P_o}{D_{\text{eff}} V_{\text{in}}} + \frac{1}{2} \frac{V_{\text{in}} L_{m1}}{L_{m1} + L_k} \left(\frac{D_{\text{eff}} T_s}{L_{m1} + L_k} \right) \tag{28}$$

where D_{eff} is the secondary-side effective duty cycle. The average current through D_o in ACCI converter is given by

$$I_{D_o,\text{avg}} = \frac{P_o}{V_o} \tag{29}$$

The voltage stresses of S_1, S_2, D_r and D_o in the proposed converter have been given in (23) and (24) respectively. The peak currents through S_1 and S_2 in the proposed converter are given by

$$I_{S_1,pk} = I_{S_2,pk} = \frac{P_o}{V_{\text{in}}} + \frac{1}{2} \frac{V_o (1 - D_2) D_2 T_s}{(n_2 + 2) L_{m2}} \tag{30}$$

The average currents through the diodes are

$$I_{D_r,\text{avg}} = I_{D_o,\text{avg}} = \frac{P_o}{V_o} \tag{31}$$

From equations (26), (28), (23) and (30), the active switch PDU ratio between the proposed converter and the ACCI converter can be calculated as

$$R_{\text{PDU\_sw}} = \frac{\text{PDU}_{\text{proposed}}}{\text{PDU}_{\text{ACCI}}} = 129\% \tag{32}$$

This equation indicates that the active switch PDU of the proposed converter is improved 29% compared to the traditional PWM ACCI converter [19].

Similarly, the diode PDU ratio of the proposed converter over ACCI converter can be calculated as

$$R_{\text{PDU\_diode}} = \frac{\text{PDU}_{\text{proposed}}}{\text{PDU}_{\text{ACCI}}} = 138\% \tag{33}$$

This means the diode PDU is improved 38%. (32) and (33) indicate that although extra diode D_r and small resonant capacitor C_r have been added into the proposed converter, the device utilization was improved, leading to reduction of the silicon area required to realize the power devices of the proposed converter.

D. ZVS of Switches and ZCS of Diodes

In order achieve ZVS of S_1 and S_2, two conditions must be satisfied. First condition is that the stored energy at the turn-off transition should be high enough to fulfill the charge and discharge equivalent capacitance Cs. Second condition is that there should be enough dead time interval for charge and discharge of C_s. As shown in Fig. 5, at S_2 turn-off instant t_0, i_{L_m}, which reaches valley point, starts to charge C_s. The condition of ZVS for S_1 is

$$\frac{1}{2} L_m i_{Lm}(t_0)^2 \geq \frac{1}{2} C_s V_{Cc}^2 \tag{34}$$

Substituting (16), (18), and (21) into (34) yields

$$L_m \left(\frac{n+2}{1-D} \frac{P_o}{V_o} - \frac{1}{2} \frac{(1-D) \cdot D}{n+2} \frac{V_o}{f_{sw} L_m} \right)^2 \geq C_s \left(\frac{V_o}{n+2} \right)^2 \tag{35}$$

The dead time requirement for achieving ZVS of S_1 is

$$\Delta t_{2\_0} = t_2 - t_0 \geq \frac{C_s V_{Cc}}{i_{Lm}(t_0)} \tag{36}$$

Substituting (16), (18), and (21) into (36) yields

$$\Delta t_{2\_0} \geq \frac{\frac{C_s V_o}{n+2}}{\frac{n+2}{1-D} \frac{P_o}{V_o} - \frac{1}{2} \frac{(1-D) \cdot D}{n+2} \frac{V_o}{f_{sw} L_m}} \tag{37}$$

As shown in Fig. 5, the condition for achieving ZCS for D_r is that i_{Dr} resonates to zero before S_2 turns on. This requires that

$$C_{\text{eq1}} \leq \left(\frac{D T_s}{\pi} \right)^2 / L_{lk} \tag{38}$$

Similarly, the condition for achieving ZCS of D_o is

$$C_{\text{eq2}} \leq \left(\frac{(1-D) T_s}{\pi} \right)^2 / L_{lk} \tag{39}$$

The definitions of C_{eq1} and C_{eq2} have been given in Section II.

E. Summary of Design Produce

A design procedure of the proposed converter according to above specifications is summarized as follows:

1) Magnetic core selection: In order to design with low profile to integrate the converter at the back side of PV module, a RM14-LP low profile core with optimized length versus area factor from Ferroxcube [32] was selected. Another advantage of RM-14-LP core is that we can design a hybrid transformer with minimized leakage inductance.
2) Transformer turns ratio: Two constraints decide the turns ratio of hybrid transformer. First constraint is from the boost ratio of (14), which should ensure the duty ratio in a reasonable range within the whole input PV voltage ranges. Second constraint is the switch device voltage stress of equation (23). For a high boost ratio converter, one of the major losses is due to the primary RMS conduction loss. In order to reduce this loss, MOSFET with low $R_{\text{ds(on)}}$ is preferred. This needs the voltage stress of the active switches, which is given by (23), to be kept under a low level.

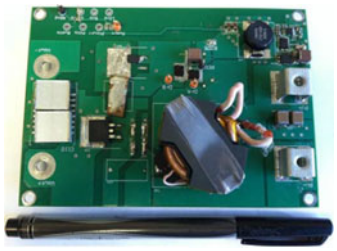

Fig. 7. Photograph of the prototype board.

TABLE II
POWER STAGE COMPONENTS SELECTION

$C_{\rm in}$	$4 \times 20\ \mu$F/100 V ceramic capacitors
Core	RM14-LP-3C95
Primary	3T of 1650/44 Litz AWG 12
Secondary	16T of 250/44 Litz AWG 20
S_1, S_2	BSB056N10NN3-G
C_r	0.4 μF film capacitors
L_m / L_{lk}	5.6 μH/4.8 μH
C_c	$2 \times 10\ \mu$F/100 V ceramic capacitors
D_r, D_o	BYV29B-500
C_o	$2 \times 1\ \mu$F/600 V film capacitors

3) Magnetizing inductance: The valley magnetizing current is utilized to achieve ZVS of the bottom switch. The ZVS condition under specific output power ranges for the bottom switch is represented by (34) and (35), which determine the requirement of magnetizing inductance.
4) Resonant capacitor C_r: The voltage rating of C_r can be decided from (15). The capacitance of $C_{\rm r}$ can be designed based the ZCS requirements output diodes, as given in (37) and (38) for specific input voltage ranges.
5) Clamping capacitor C_c: The clamping capacitor C_c should be selected such that the voltage ripple on C_c is kept to a negligibly low level.

IV. EXPERIMENTAL VERIFICATIONS

In order to verify the effectiveness of the proposed converter, a prototype circuit with the photograph shown in Fig. 7 was built and tested. Table II lists the power stage components selection for the proposed converter designed with a 250-W rated power. In the experiment, the prototype converter was designed to convert the low input voltage $V_{\rm in}$ from PV module with the voltage varying from 20 to 45 V to a constant high dc-bus voltage 380 V. To achieve final low profile design, we design the transformer with low profile magnetic core RM14-LP. Due to the increased boost gain as calculated in (14) as compared to traditional coupled-inductor based PWM converters, we can decrease the turns ratio of the transformer, allowing optimal utilization of the window area of the magnetic core. This is beneficial to low-profile type cores, since they normally have smaller window area compared to the regular counterparts.

Fig. 8 highlights the experimental waveforms of driver signal of S_1, input current i_p and drain–source voltage of S_1 with $V_{\rm in} = 30$ V, $P_o = 220$ W and $V_o = 380$ V. As seen from Fig. 8, the switch voltage stress is kept at a low level; the input current

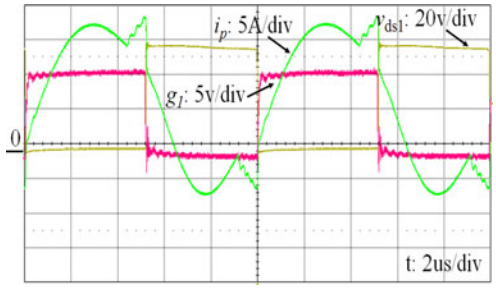

Fig. 8. Experimental waveforms: driver single of S_1, input current i_p, and drain–source voltage of S_1: ($V_{\rm in} = 30$ V, $P_o = 220$ W).

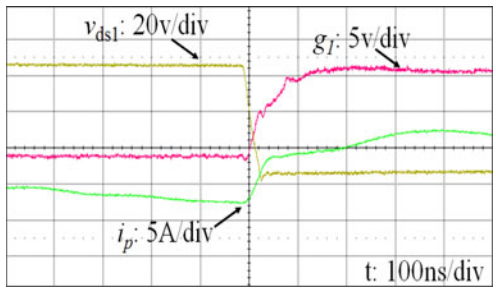

Fig. 9. Waveforms indicating ZVS of main switch S_1.

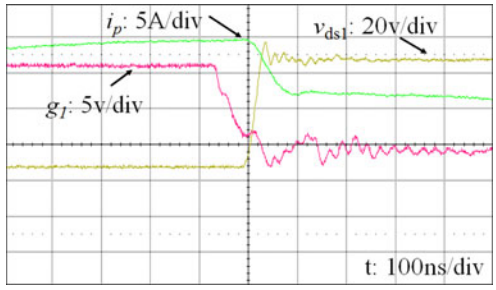

Fig. 10. Waveforms indicating ZVS of auxiliary switch S_2.

is composed of sinusoidal resonant and linear PWM currents, illustrating hybrid resonant and PWM power conversion. This hybrid operation improves the utilization of magnetics. The resonant portion of the primary current resonates back to zero at both on and off periods of the main switch. This helps ZCS turn-off of both resonant and output diodes. When S_1 turns off, the primary side current is at the peak point, which helps S_2 achieving ZVS turn on. However when S_1 turns on, the primary side current is at the valley point, which helps S_1 achieving ZVS turn on.

Fig. 9 shows the zoom-in waveforms indicating ZVS of main switch S_1. It can be seen when S_1 is turned, the drain–source voltage of S_1 has reached to zero, illustrating the ZVS turn on of S_1.

Fig. 10 shows the zoom-in waveforms indicating ZVS of auxiliary switch S_2. It can be seen that main switch S_1 is turned off by the driver g_1 within the "Miller Plateau." With the positive current i_p, S_2 can be turned on with ZVS after dead time.

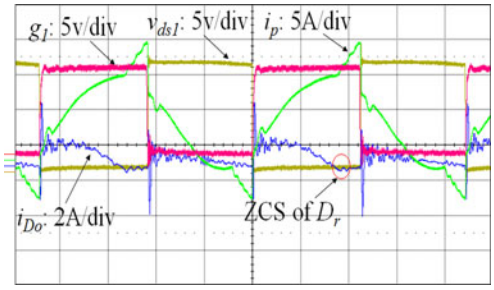

Fig. 11. Experimental waveforms indicating ZCS of D_r: $V_{\rm in} = 30$ V, $P_o = 150$ W.

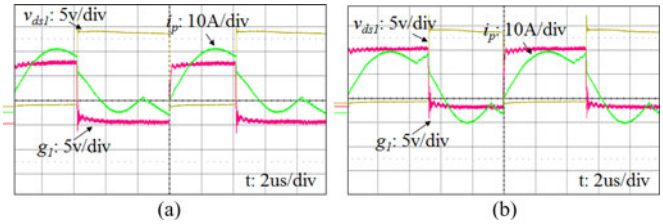

Fig. 12. Experimental waveforms for different operations: (a)$V_{\rm in} = 35$ V, $P_o = 250$ W; and (b) $V_{\rm in} = 30$ V, $P_o = 250$ W.

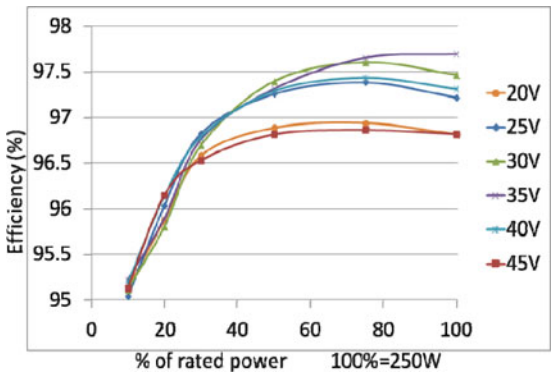

Fig. 13. Measure efficiency.

Fig. 11 shows the experimental waveforms of driver signal of S_1, input current i_p and drain–source voltage of S_1 and the current $i_{\rm Dr}$ with $V_{\rm in} = 30$ V, $P_o = 175$ W and $V_o = 380$ V. $i_{\rm Dr}$ resonant back to zero before the turn on of S_2 highlights the ZCS turn off of D_r.

More experimental waveforms are shown in Fig. 12 with different operation conditions (a) $V_{\rm in} = 35$ V, $P_o = 250$ W, and (b) $V_{\rm in} = 30$ V, $P_o = 250$ W.

Fig. 13 summarizes the conversion efficiencies for different input voltages under different percent output power levels. All the conversion efficiencies from 10% to 100% output power are higher than 95% and the peak efficiency is 97.7% under 35 V input with 250 W output power level. Fig. 14 gives the weighted CEC efficiencies for different input voltages according following equation:

$$\eta_{\rm CEC} = 0.04\eta_{10\%} + 0.05\eta_{20\%} + 0.12\eta_{30\%} + 0.21\eta_{50\%} + 0.53\eta_{75\%} + 0.05\eta_{100\%} \quad (40)$$

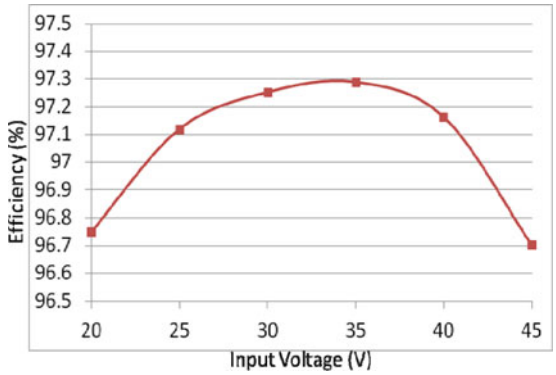

Fig. 14. Calculated CEC efficiency versus input voltages.

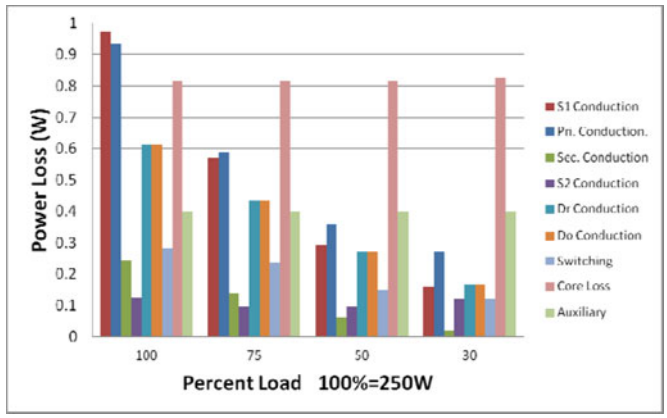

Fig. 15. Individual losses over% load.

As seen from Fig. 14, the CEC efficiencies over the 20 to 45 V input voltage range were over 96.7% due to the relatively flat conversion efficiency curves for all input voltages as shown in Fig. 13. The maximum CEC efficiency voltage range is from 25 to 40 V, which matches the MPPT regions in the PV module *I–V* curves shown in Fig. 1. This feature is very desirable because it ensures maximum energy capture from the PV modules.

Fig. 15 shows the individual power losses at different percent output power levels at 30 V input voltage. As it can be seen from Fig. 15, one of the dominant losses is the primary conduction losses due to the relatively high input RMS current. Because of the low dc-bias of the magnetizing current, primary side of transformer can use less turns, while still avoiding saturation of magnetic core. This allows to effectively reduce the primary conduction losses. Since the voltage-second on the transformer is same for different output power, the core loss keeps constant. However, this hurts the converter efficiency at light load conditions. The control strategy which can optimize the light load efficiency will be reported in future work. The auxiliary losses represent the losses from those other than the main power stage, such as housekeeping loss. These losses are insensitive to the output power and almost keep constant.

V. Conclusions

A high boost ratio ZVS/ZCS PV module integrated dc–dc converter with hybrid transformer is presented. By incorporating

resonant operation mode into traditional high boost ratio active-clamp coupled-inductor PWM converter, the proposed converter obtains the following features and benefits:

1) ZVS turn-on of active switches and ZCS turn-off of diodes, reducing the switching losses and EMI noises;
2) fixed low voltage stresses for all power devices at steady-state operations, independent of wide changing input PV module voltage;
3) the MU is optimized as a result of energy transfer to the high voltage side throughout the whole switching period, allowing utilization of smaller-size magnetics and low-profile design;
4) continuous input current with combined resonant and PWM waveforms reducing the RMS conduction losses;
5) flat efficiency curves leading to high CEC efficiency over wide input voltage range;
6) elimination of lossy snubber circuit for output diodes;
7) although an additional resonant diode and a small resonant capacitor are added, the total PDU is improved;
8) the input voltage region with high CEC efficiencies matches the PV module maximum power point ranges, achieving maximum energy yield.

A prototype circuit targeted for PV module integration with 20–45 V input voltage range and 380 V dc output was built and tested. The test CEC efficiencies including the driver and auxiliary power supply losses are higher than 96.7% from 20 to 45 V input voltages. Due to the simple structure, easy to control, low profile design and high CEC efficiency over wide input voltage and output power ranges, the proposed converter is very attractive to work as a PV module integrated converter.

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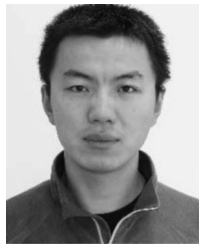

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