Modeling, Design and Fault Analysis of Bidirectional DC-DC Converter for Hybrid Electric Vehicles

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***Abstract*—This paper presents modeling, design and analysis of a bidirectional half-bridge DC/DC converter suitable for power electronic interface between the main energy storage system and the electric traction drive in hybrid electric vehicles. A hybrid energy storage system composed of a battery unit and an ultracapacitor pack is considered. A parallel dc-linked multi-input converter with a half-bridge bidirectional DC/DC cell topology is chosen to link the battery/ultracapacitor storage unit with the dc-link. The paper focuses on modeling the proposed converter for both dynamic and steady state analysis. Averaging and linearization techniques are applied to obtain the averaged state space models and small signal models of the converter in both boost and buck operation modes. A criterion for sizing the converter passive components based on the imposed design specifications and constraints is illustrated. Simulation results of the buck-boost converter during normal functioning and under faulty conditions are presented. In particular, short-circuit faults and open-circuit faults of diodes and transistors are analyzed.**

Keywords—Bidirectional DC/DC converter; hybrid electric vehicles; dynamic modeling; state space representation; components sizing; design; simulation; fault analysis

I. INTRODUCTION

The use of DC/DC converters is essential in hybrid vehicles. Mainly, there exist two types of DC/DC converters onboard of a Hybrid Electric Vehicle (HEV). The first is a low power bidirectional DC/DC converter which connects the high voltage dc-link with a low voltage battery used to supply low power loads. The second is a high power bidirectional DC/DC converter used to connect the main energy storage unit with the electric traction drive system [1]. This paper presents modeling, design and analysis of the later converter. A Hybrid Energy Storage System (HESS) composed of a battery unit and an UltraCapacitor (UC) pack is considered. Based on the study done in [2], a parallel dc-linked multi-input converter with half-bridge bidirectional DC/DC cells is chosen to link the battery/UC storage unit with the dc-link. The DC/DC converter is used to provide a regulated dc voltage at higher level to the inverter and to control power flow to and from the electric drive during motoring and generating modes respectively. The paper mainly focuses on modeling the proposed converter for both dynamic and steady state analysis. Section II describes the electric drive train specifications. In Section III, averaging and linearization techniques are applied to the DC/DC converter state space model for both boost and buck operation modes. A criterion for sizing the converter passive components based on the imposed design constraints is presented in Section IV. Section V presents simulation results of the chosen converters using Matlab/Simulink. The operation of the buck-boost converter is illustrated during normal functioning and under faulty conditions resulting from power switching device faults. In particular, Short-Circuit (SC) and Open-Circuit (OC) faults of diodes and transistors are analyzed. A single fault is carried at a time; leading to eight different fault operation modes.

II. ELECTRIC TRACTION SYSTEM SPECIFICATIONS

When designing a bidirectional DC/DC converter suitable for Power Electronic Interface (PEI) between the Energy Storage System (ESS) and the electric traction drive, it is important to indicate the specifications of the electric traction system. These specifications include identifying the level of hybridization of the vehicle; as well as the choice of hybrid drive train configuration, HESS, electric AC drive system, and DC/DC PEI configuration.

A. Level of Hybridization

In order to determine the dc-link voltage and the energy storage unit capacity at the DC/DC converter terminals, it is empirical to specify the vehicle hybridization level. A full HEV is chosen with large traction motor, high-capacity energy storage pack and main DC bus voltage around 200-300V.

B. Choice of Hybrid Drivetrain Configuration

A parallel hybrid drive train rather than a series one is chosen for several reasons. As shown in Fig.1, the vehicle can be driven by the ICE alone, the EM alone or both engines at the same time utilizing the best performance of each. Unlike series hybrids, parallel hybrids require less number of energy conversion stages and feature less power demands on the electrical system which makes parallel hybrids less expensive and more energy efficient.

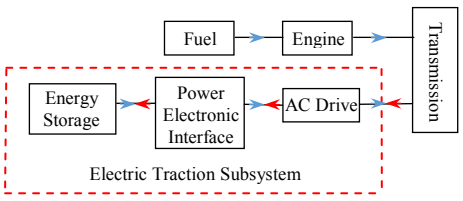


Fig. 1. Parallel hybrid drivetrain configuration

C. Choice of Hybrid Energy Storage System

HEVs rely on the capability of their ESSs not only to store large amounts of energy but also to discharge according to load demand. A high power, high energy, and high efficiency ESS can be obtained by utilizing a hybrid battery/UC combination. The UC will increase the ESS power handling capability and reserve the amount of regenerative energy dissipated in the friction brakes due to the low power handling capability of the battery. The UC is used during transient peak power demands and to capture regenerative energy which greatly reduces the voltage variations and stresses across the battery terminals and releases the burden of power converter interfacing the battery.

D. Choice of Electric AC Drive System

The AC drive is a classic Permanent Magnet Synchronous Motor (PMSM) drive which consists of a PMSM, a three-phase bridge voltage source inverter and a power electronic controller. Voltage source inverters are commonly used in HEV applications, where the source delivers a stiff voltage. PMSMs exhibit higher efficiency, higher power density and higher torque-to-inertia ratio when compared to induction motors. These advantages as well as the fast torque response make PMSMs good candidates for use in HEVs. The main disadvantage is the use of permanent magnets which are not only expensive but also sensitive to load and temperature.

E. Choice of Power Electronics Interface Configuration

To get full control over the power flowing to and from the battery and to limit the fluctuating voltage levels at the UC terminals, it is necessary to utilize a DC/DC PEI between the storage units and the AC drive. The choice of a power converter as simple yet as efficient as possible to interface the HESS is discussed in [2]. Accordingly, a parallel dc-linked multi-input bidirectional converter is chosen as shown in Fig. 2. The proposed multi-input bidirectional DC/DC converter interfacing the battery/UC HESS and the traction drive in the HEV consists of two bidirectional half-bridge cells as shown in Fig. 3. Each half-bridge cell consists of an energy storage element (inductor), two IGBT power transistors, and two diodes for bidirectional current flow. IGBTs are chosen since they are suitable for low frequency, high power applications such as the full hybrid vehicle considered. An input capacitor interfacing the source acts as a filter limiting the source current ripple and the circulation of high-frequency components through the sources. This filtering is mainly used due to the Equivalent Series Resistance (ESR) of each of the battery and UC pack. Finally, one common output capacitor is shared between the two cells to minimize the voltage ripple at the DC bus and the inverter input terminals while the battery and UC voltages remain at a level lower than that of the dc-link.

III. Dynamic Modeling of Proposed Bidirectional DC/DC Converter

Dynamic modeling of power converter is necessary in order to study its transient behavior and analyze how variations in the input voltage, load current, and duty cycle affect its output voltage [3]-[15]. However, a switching power converter is a nonlinear time-varying system which is difficult to analyze due to its intrinsic large signal nature. Small signal modeling is a commonly used approach to simplify the analysis, control and design of the converter nonlinear system by transforming it into a linear time-invariant system. This is usually done by taking the average value of the state variables over one switching period and is known as state space averaged modeling which enables analyzing the system dynamic behavior. The converter state space equations are used to derive the small signal averaged equations and the system transfer functions which are further used in the design of the controllers to regulate the system performance. Fig. 4 shows the switching power converter model. The converter state variables are the capacitors voltages, v_{Cin} and v_{Co}, and inductor current, i_L. The input variables are the load current, i_o, and the input source voltage, v_{in} for battery or UC. The output variable is the dc-link voltage, v_o, for UC fed converter and the source current, i_{in}, for battery fed converter.

The half-bridge converter is bidirectional in current; thus, it is analyzed once as a boost converter stepping up voltage from the battery/UC to the load side and then as a buck converter stepping down voltage from the dc-link to the source. The half-bridge converter never operates in discontinuous conduction mode due to the fact that the power devices (T1 with D2 and T2 with D1) function in complementary modes and have bidirectional load and source. This fact reduces current peaks as well as stresses on passive and active components. Moreover, the half-bridge converter switches function pair-wise, meaning that when T1 is ON, T2 is OFF, and vice versa. If both transistors lead at the same time there is a SC and risk of destroying components. Thus, the converter always operate in continuous conduction mode with only two switching states for each of the boost and buck operations as shown in Table I.

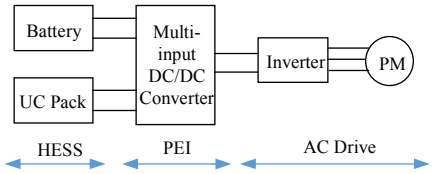


Fig. 2. Electric drive subsystem

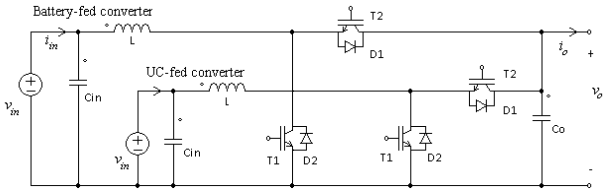


Fig. 3. Parallel dc-linked multi-input bidirectional DC/DC converter

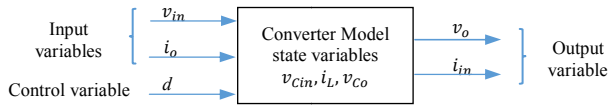


Fig. 4. Power switching converter model

TABLE I. Switching Configurations of Half-Bridge Converter

Switching State	T1	D1	T2	D2	Power Flow
Boost mode 1	ON	OFF	OFF	OFF	Source to Load
Boost mode 2	OFF	OFF	OFF	ON	Source to Load
Buck mode 1	OFF	OFF	ON	OFF	Load to Source
Buck mode 2	OFF	ON	OFF	OFF	Load to Source

A. Converter Averaged State Space Representation

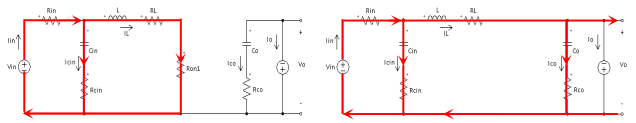
A mathematical model of the converter during boost and buck operations can be obtained by applying Kirchhoff's voltage and current equations for each of the commutation modes shown in Fig. 5 and Fig. 6 respectively. The parasitic resistances of all power inductors and capacitors, the transistors ON resistances and the storage unit ESR are included. During buck operation, the currents shown on Fig. 6 are negative.

The converter averaged state space equations are obtained by taking a linearly weighted average of the equations in both switching modes using the duty cycle as control variable with

$$\dot{x} = \mathrm{A}x + \mathrm{B}u \tag{1}$$

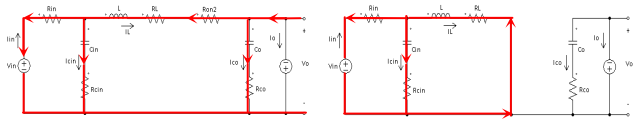
$$y = \mathrm{C}x + \mathrm{E}\dot{x} + \mathrm{F}u$$

where $x = \begin{bmatrix} v_{Cin} \\ i_L \\ v_{Co} \end{bmatrix}$ is the state space vector, $u = \begin{bmatrix} v_{in} \\ i_o \end{bmatrix}$ is the input or control vector and $y = [v_o]$ is the output vector for the UC fed converter while $y = [i_{in}]$ for the battery fed converter. A, B, C, E, and F are the averaged matrices given by $\mathrm{A} = \mathrm{A}_1 d + \mathrm{A}_2(1-d)$, $\mathrm{B} = \mathrm{B}_1 d + \mathrm{B}_2(1-d)$, $\mathrm{C} = \mathrm{C}_1 d + \mathrm{C}_2(1-d)$, $\mathrm{E} = \mathrm{E}_1 d + \mathrm{E}_2(1-d)$, and $\mathrm{F} = \mathrm{F}_1 d + \mathrm{F}_2(1-d)$. Indices 1 and 2 refer to the matrices obtained during commutation modes 1 and 2. d is the converter duty cycle, defined as the ratio of transistor ON time to switching period T_s, with $d = d_{boost} = t_{T1ON}/T_s$ during boost operation and $d = d_{buck} = t_{T2ON}/T_s$ during buck. d is used as a control variable which appears inside the averaged matrices expression rather than in the input vector u. Matrices A and B remain the same for both UC and battery fed converters since they depend on circuit modeling as given below. For the UC fed converter, $C_{boost1} = [0 \quad 0 \quad 1]$, $C_{boost2} = [0 \quad R_{Co} \quad 1]$, $E_{boost1} = E_{boost2} = [0 \quad 0 \quad 0]$ and $F_{boost1} = F_{boost2} = [0 \quad -R_{Co}]$. $C_{buck1} = [0 \quad R_{Co} \quad 1]$, $C_{2buck} = C_{2buck} = [0 \quad 1 \quad 0]$, $E_{buck1} = E_{buck2} = [C_{in} \quad 0 \quad 0]$ and $F_{buck1} = F_{buck2} = [0 \quad 0]$. Using the above matrices, the averaged state space equations of the UC and battery fed converters during boost and buck operations can be calculated.



(a) boost mode 1 (b) boost mode 2

Fig. 5. Boost converter normal operation modes



(a) buck mode 1 (b) buck mode 2

Fig. 6. Buck converter normal operation modes

B. Converter Steady State Equations

During steady state, the averaged inductor voltage over one switching period is zero; therefore, at steady state $\langle v_L \rangle_{avg} = 0$ and $\langle \frac{di_L}{dt} \rangle_{avg} = 0$. This is known as the principle of inductor-volt second balance. Similarly, the principle of capacitor charge balance states that the steady state averaged capacitor current over one switching period is zero, so $\langle i_{Co} \rangle_{avg} = \langle i_{Cin} \rangle_{avg} = 0$ and $\langle \frac{dv_{Co}}{dt} \rangle_{avg} = \langle \frac{dv_{Cin}}{dt} \rangle_{avg} = 0$. Substituting $\dot{X} = 0$ in (1) results in the average values over one switching cycle in steady state of each of the state variables, V_{Cin}, I_L, and V_{Co}, and the output variables, V_o, I_L, and I_{in}, in terms of the input variables, V_{in} and I_o, and the duty cycle d given by

$$X = -\mathrm{A}^{-1}\mathrm{B}U \tag{2}$$

$$Y = \left(-\mathrm{C}\mathrm{A}^{-1}\mathrm{B} + \mathrm{F}\right)U$$

C. Small Signal Model

To obtain the small signal model equations from the state space equations, the state variables, output variables and duty cycle as a control variable will be split into their steady state average DC values represented by upper case variables plus a small AC variation about the average values represented by lower case variables with a caret on top given by $x = X + \hat{x}$, $y = Y + \hat{y}$, and $d_1 = D_1 + \hat{d}_1$ respectively, resulting in

$$\dot{\hat{x}} = \mathrm{A}\hat{x} + \mathrm{B}\hat{u} + \{(\mathrm{A}_1 - \mathrm{A}_2)X + (\mathrm{B}_1 - \mathrm{B}_2)U\}\hat{d} \tag{3}$$

$$\hat{y} = \mathrm{C}\hat{x} + \mathrm{E}\dot{\hat{x}} + \mathrm{F}\hat{u} + \{(\mathrm{C}_1 - \mathrm{C}_2)X + (\mathrm{F}_1 - \mathrm{F}_2)U\}\hat{d}$$

Applying Laplace transform to (3) results in the converter small signal transfer functions. Usually, the most important transfer functions are variations in the output variables, $\hat{v}_o$ or $\hat{\imath}_{in}$, to variations in the duty cycle, $\hat{d}$, as a control variable. Accordingly, for the UC fed converter, the v_o is the output with $\left.\frac{\hat{v}_o(s)}{\hat{d}(s)}\right|_{\hat{u}(s)=0} = \mathrm{C}[sI - \mathrm{A}]^{-1}[(\mathrm{A}_1 - \mathrm{A}_2)X + (\mathrm{B}_1 - \mathrm{B}_2)U] + (\mathrm{C}_1 - \mathrm{C}_2)X$. For the battery fed converter, i_{in} is the output variable with $\left.\frac{\hat{\imath}_{in}(s)}{\hat{d}(s)}\right|_{\hat{u}(s)=0} = \{[\mathrm{C} + \mathrm{EA}][sI - \mathrm{A}]^{-1} + \mathrm{E}\}[(\mathrm{A}_1 - \mathrm{A}_2)X + (\mathrm{B}_1 - \mathrm{B}_2)U]$.

$$\mathrm{A}_{1boost} = \begin{bmatrix} -\frac{1}{C_{in}R_{iCin}} & -\frac{R_{in}}{C_{in}R_{iCin}} & 0 \\ \frac{R_{in}}{LR_{iCin}} & -\frac{(R_{in}R_{Cin}+R_LR_{iCin}+R_{ON1}R_{iCin})}{LR_{iCin}} & 0 \\ 0 & 0 & 0 \end{bmatrix}, \mathrm{A}_{2boost} = \begin{bmatrix} -\frac{1}{C_{in}R_{iCin}} & -\frac{R_{in}}{C_{in}R_{iCin}} & 0 \\ \frac{R_{in}}{LR_{iCin}} & -\frac{(R_{in}R_{Cin}+R_LR_{iCin}+R_{Co}R_{iCin})i_L}{LR_{iCin}} & -\frac{1}{L} \\ 0 & \frac{1}{C_o} & 0 \end{bmatrix}, \mathrm{B}_{1boost} = \begin{bmatrix} \frac{1}{C_{in}R_{iCin}} & 0 \\ \frac{R_{Cin}}{LR_{iCin}} & 0 \\ 0 & -\frac{1}{C_o} \end{bmatrix}, \text{and } \mathrm{B}_{2boost} = \begin{bmatrix} \frac{1}{C_{in}R_{iCin}} & 0 \\ \frac{R_{Cin}}{LR_{iCin}} & \frac{R_{Co}}{L} \\ 0 & -\frac{1}{C_o} \end{bmatrix}.$$

$$\mathrm{A}_{1buck} = \begin{bmatrix} -\frac{1}{C_{in}R_{iCin}} & -\frac{R_{in}}{C_{in}R_{iCin}} & 0 \\ \frac{R_{in}}{LR_{iCin}} & -\frac{(R_{in}R_{Cin}+R_LR_{iCin}+R_{ON2}R_{iCin}+R_{Co}R_{iCin})}{LR_{iCin}} & -\frac{1}{L} \\ 0 & \frac{1}{C_o} & 0 \end{bmatrix}, \mathrm{A}_{2buck} = \begin{bmatrix} -\frac{1}{C_{in}R_{iCin}} & -\frac{R_{in}}{C_{in}R_{iCin}} & 0 \\ \frac{R_{in}}{LR_{iCin}} & -\frac{(R_{in}R_{Cin}+R_LR_{iCin})}{LR_{iCin}} & 0 \\ 0 & 0 & 0 \end{bmatrix}, \mathrm{B}_{1buck} = \begin{bmatrix} \frac{1}{C_{in}R_{iCin}} & 0 \\ \frac{R_{Cin}}{LR_{iCin}} & \frac{R_{Co}}{L} \\ 0 & -\frac{1}{C_o} \end{bmatrix}, \text{and } \mathrm{B}_{2buck} = \begin{bmatrix} \frac{1}{C_{in}R_{iCin}} & 0 \\ \frac{R_{Cin}}{LR_{iCin}} & 0 \\ 0 & -\frac{1}{C_o} \end{bmatrix}.$$

IV. CONVERTER DESIGN PARAMETERS

To satisfy the electric traction power demand of a full HEV, the converter is rated at 30kW output power. Voltage, current and power ratings are based on the requirements of an HEV with 300V-30kW dc-link. Practical switching frequencies for power switching converters used in HEVs fall in the range of 15-20kHz. An energy source of 200V is considered at the input of the DC/DC converter. The passive components are sized based on the ripple requirements specified in Table II.

The inductor size can be determined by considering the constraint on Δi_L either during boost or buck operation. Usually, Δi_L is chosen to be 10-15% of the maximum DC average inductor current, $I_{L_{avg}}$, which can be determined from the averaged steady state model as $I_{L_{avg}} = \frac{I_{link}}{1-d_{boost}} = 150\text{A}$ where $d_{boost} = 1 - \frac{v_{source}}{v_{link}} = 0.33$. Considering the converter during boost mode 1, the slope of the inductor current waveform is given by $\frac{di_L}{dt} = \frac{v_L}{L} = \frac{2\Delta i_L}{d_{boost}T_s}$. Ignoring the parasitic resistances, v_L is estimated by v_{source} and the inductor size is given by

$$L = \frac{d_{boost}v_{source}}{2\Delta i_L f_s} = 146.67\mu\text{H} \quad (4)$$

The inductor current which consists of a DC average component, I_L, and an AC ripple component, Δi_L, is considered again when determining the sizes of the input capacitor, C_{in}, and output capacitor, C_o. During boost operation, the inductor current DC component must flow exclusively through the dc-link. Whereas, Δi_L is prefered to flow through C_o instead of the dc-link; therefore, the steady state current $I_{Co} = \Delta i_L$. C_{in} is sized to reduce the output voltage ripple, Δv_o, which is chosen to be 4.5% of the maximum average dc-link voltage. By setting $\Delta v_{R_{Co}} = \Delta v_o$, an upper bound of the ESR of C_o is given by $R_{Co_{max}} = \frac{\Delta v_o}{\Delta i_L} = 0.9\Omega$. During boost mode 2, the slope of the capacitor voltage waveform is $\frac{dv_{Co}}{dt} = \frac{I_{Co}}{C_o} = \frac{2\Delta v_{Co}}{(1-d_{boost})T_s}$. By setting $\Delta v_{Co} = \Delta v_o$, a lower bound of the output capacitance is given by $C_{o_{min}} = \frac{(1-d_{boost})\Delta i_L}{2\Delta v_o f_s} = 248\text{mF}$. In fact, a more accurate limit of C_o based on the choice of R_{Co} is found using

$$C_o = \frac{(1-d_{boost})\Delta i_L}{2(\Delta v_o - \Delta i_L R_{Co})f_s} \quad (5)$$

Similarly during buck operation, I_L must flow exclusively through the source; whereas, Δi_L must flow through C_{in}; therefore, at steady state $I_{Cin} = \Delta i_L$. C_{in} is sized to reduce the voltage ripple at the source side, Δv_{in}, which is limited to be 2% of the maximum nominal source voltage. By setting $\Delta v_{R_{Cin}}$ equal to Δv_{in}, an upper bound of the ESR of C_{in} is given by $R_{Cin_{max}} = \frac{\Delta v_{in}}{\Delta i_L} = 0.267\Omega$. Using the capacitor charge equation $\Delta v_{Cin} = \frac{\Delta Q}{C_{in}}$, where $\Delta Q = \frac{1}{2}\Delta i_L \frac{T_s}{2}$ is obtained from the capacitor current waveform during steady state, the input capacitance is $C_{in} = \frac{\Delta i_L}{4f_s \Delta v_{Cin}}$. By setting $\Delta v_{Cin} = \Delta v_{in}$, a lower bound of C_{in} is found to be $C_{in_{min}} = \frac{\Delta i_L}{4f_s \Delta v_{in}} = 62.5\mu\text{F}$. A more precise value of C_{in} can be obtained based on the choice of R_{Cin} by

$$C_{in} = \frac{\Delta i_L}{4f_s(\Delta v_{in} - \Delta i_L R_{Cin})} \quad (6)$$

V. SIMULATION RESULTS

To verify the converter operation, the proposed design is simulated using Matlab/Simulink based on the parameters specified in Table II and Table III. The operation of the buck-boost converter is illustrated during normal functioning and under faulty conditions resulting from power switching device faults. SC and OC faults of the converter diodes and transistors are analyzed. A single fault is carried at a time; leading to eight different fault operation modes as shown in Table IV.

A. Boost Converter

During boost operation, power flows from the energy source modeled as a voltage source rated at 200V-30kW in series with an internal resistance to the dc-link which is modeled as a current source rated at 300V-30kW drawing an average current of 100A from the converter.

1) Normal operation

Fig. 5 shows the current flow direction during normal operation modes of boost converter. During mode 1, *L* stores

TABLE II. DESIGN PARAMETERS

Source voltage V_{source}	200V
DC-link voltage V_{link}	300V
Rated Power P_{rated}	30kW
Source current I_{source}	150A
DC-link current I_{link}	100A
Switching frequency f_s	15kHz
Source voltage ripple Δv_{in}	2% peak-to-peak
DC-link voltage ripple Δv_o	4.5% peak-to-peak
Inductor current ripple Δi_L	±10%

TABLE III. BIDIRECTIONAL DC/DC CONVERTER PARAMETERS

Parameter	Symbol	Value
Input Capacitance	C_{in}	80µF
Input Capacitor ESR	R_{Cin}	100mΩ
Inductance	L	146µH
Inductor ESR	R_L	5mH
Output Capacitance	C_o	5mF
Output Capacitor ESR	R_{Co}	80mΩ
Transistor ON resistance	R_{ON}	1mΩ

TABLE IV. BOOST CONVERTER FAULT OPERATION MODES

Operation	Fault Mode	D2	T1	D1	T2
Boost	**1**	SC	Normal	OFF	OFF
	2	OC	Normal	OFF	OFF
	3	Normal	SC	OFF	OFF
	4	Normal	OC	OFF	OFF
Buck	**5**	OFF	OFF	SC	Normal
	6	OFF	OFF	OC	Normal
	7	OFF	OFF	Normal	SC
	8	OFF	OFF	Normal	OC

energy flowing from the source. During mode 2, the energy stored in L is transferred to the load side through D2. Fig. 7 illustrates the boost converter simulation results. The inductor current waveform shows a 150A average DC component with ± 15A current ripple. Δv_o is 4.5% of the average output dc-link voltage which also agrees with the design constraints.

2) Fault mode 1

The SC diode results in a significant increase in the current drawn from the source as show in Fig. 9. The dc-link modeled as a current source limits the current drawn from the converter to 100A. However, when T1 is ON, no current flows to the dc-link; instead the source current and the output capacitor discharge current flow through T1 resulting in a very high current which could damage the transistor.

3) Fault mode 2

When D2 is OC, the dc-link is isolated from the source. A significant decrease in the inductor current DC component is observed with $I_L = I_{T1}$ shown in Fig. 11. When T1 is ON, the source current cycles through the transistor. At the instance T1 turns OFF, the current drawn from the source cuts nearly to zero and a very high voltage spike is observed across T1 and the OC diode. These high voltage spikes could damage the power switching components in the converter.

4) Fault mode 3

Fault mode 3 causes a very high constant current to freewheel through the inductor and the short-circuited transistor with $I_{in} = I_L = I_{T1} = \frac{V_{source}}{R_{in}+R_L} = 13.33$kA. No current reaches from the source to the dc-link.

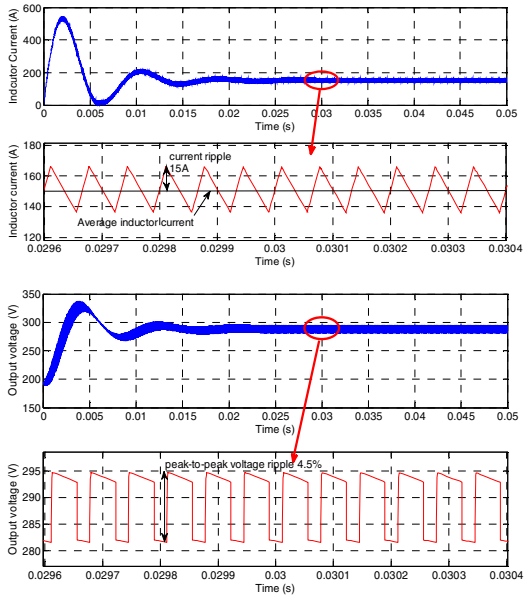
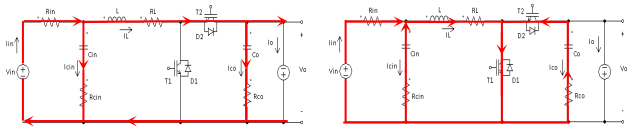


Fig. 7. Current and voltage waveforms during boost normal operation



(a) T1 OFF; D2 short (b) T1 ON; D2 short

Fig. 8. Fault 1 operation mode

5) Fault mode 4

When T1 is OC, the dc-link is directly connected to the source through L and D2. The circuit does not function anymore as a boost converter. Simulations reveal a decrease in the converter output voltage and the inductor current. The RC_{in} and RC_o branches act as open-circuits at steady state.

B. Buck Converter

During normal buck operation, power flows from the electric drive now modeled as a voltage source rated at 300V-

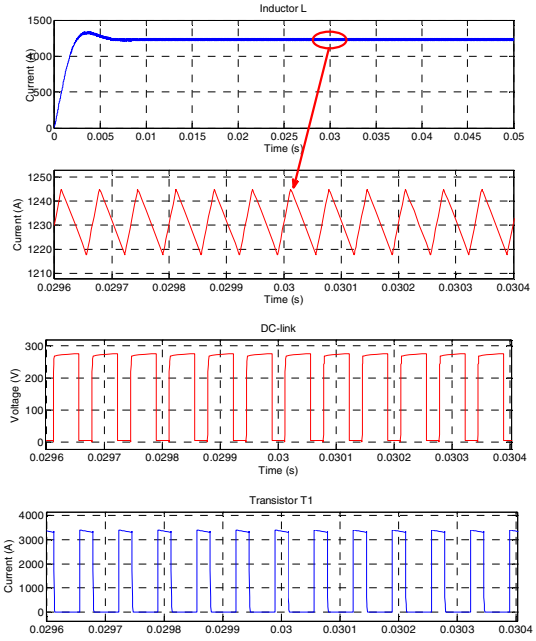
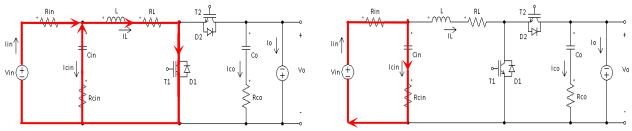


Fig. 9. Boost converter current and voltage waveforms during fault mode 1



(a) T1 ON; D2 open (b) T1 OFF; D2 open

Fig. 10. Fault 2 operation mode

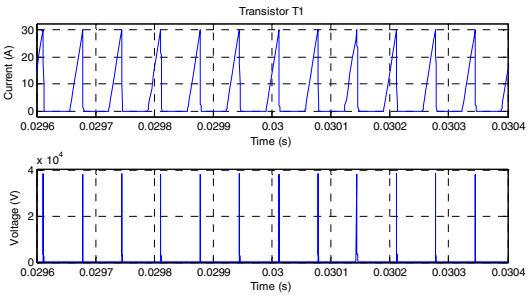


Fig. 11. T1 current and voltage waveforms during fault mode 2

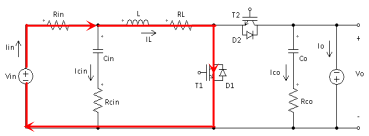


Fig. 12. Fault 3 operation mode

30kW to the energy source modeled as a resistive load rated at 200V-30kW drawing an average current of 150A from the dc-link. On the other hand, during faulty operation, the storage unit is modeled as a voltage source with ESR rather than as a resistive load, due to the fact that it has a constant DC voltage across its terminals regardless of the converter operation. The storage unit is set at 85% state of charge, 170V, which greatly affects the converter parameters during faulty conditions.

1) Normal operation

Fig. 6 shows the current flow during normal buck operation modes. Fig. 15 illustrates the buck converter simulation results. The inductor average current is 150A with ±15A ripple variation. The source DC value is 200V with 2% voltage ripple which agrees with the design constraints imposed.

2) Fault mode 5

Fault mode 5 causes a SC across the dc-link and storage unit terminals as shown in Fig. 16. A large burst of current is drawn from the dc-link through T2 to the SC diode. The transistor 1Ω ON resistance is connected alone across the 300V dc-link thus drawing a current of 300kA which can damage the transistor. No current reaches the source side from the dc-link; however, a large burst of current is drawn from the storage unit through L to the SC diode with $I_L = \frac{V_{source}}{R_{in}+R_L} = 11.33\text{kA}$.

3) Fault mode 6

When T2 is ON, the current flows from the dc-link with a significant decrease in the average value I_L. The reduced inductor current divides through the input capacitor and the source. When T2 turns OFF, no current reaches the source from the dc-link; the input capacitor discharges through the source as shown in Fig. 17 (b) and a very high voltage spike is observed across the transistor terminals as shown in Fig. 18. These voltage spikes could damage the power transistor.

4) Fault mode 7

In Fig. 19, T2 is SC. The circuit does not function as a buck converter; instead, the storage unit is directly connected to the dc-link drawing a current $I_{link} = \frac{V_{link}-V_{source}}{R_{in}+R_L} = 8.67\text{kA}$.

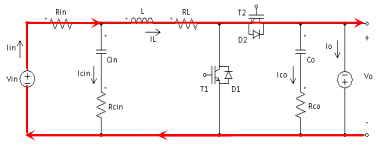


Fig. 13. Fault 4 operation mode

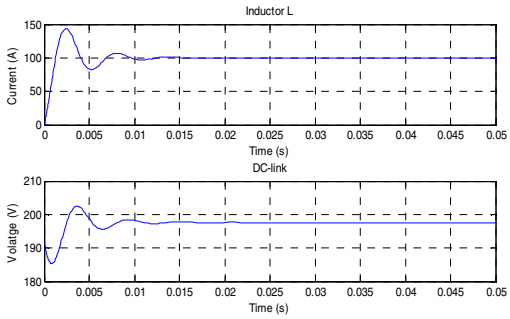


Fig. 14. Boost converter current and voltage waveforms during fault mode 4

5) Fault mode 8

When T2 is OC, the source side is completely disconnected from the dc-link. No current flows through any of the converter components.

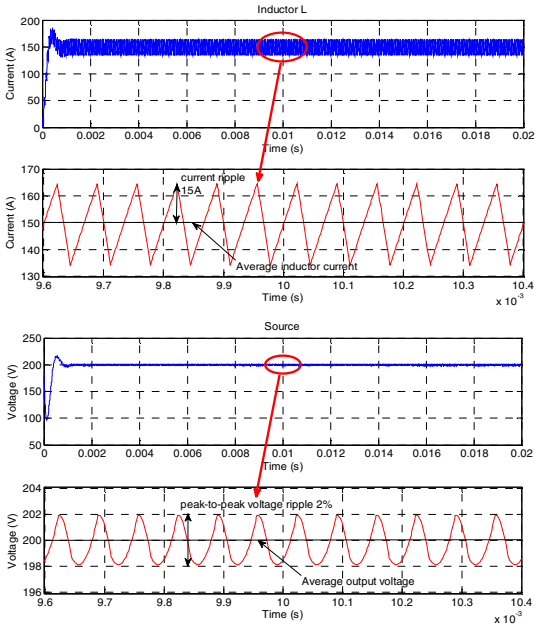


Fig. 15. Current and voltage waveforms during buck normal operation

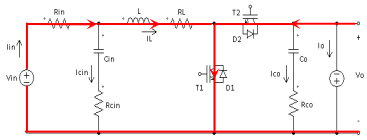
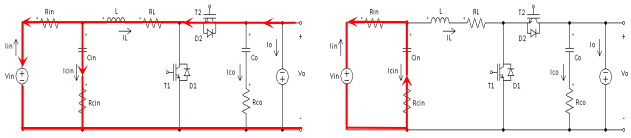


Fig. 16. Fault 5 operation mode



(a) T2 ON; D1 open (b) T2 OFF; D1 open

Fig. 17. Fault 6 operation mode

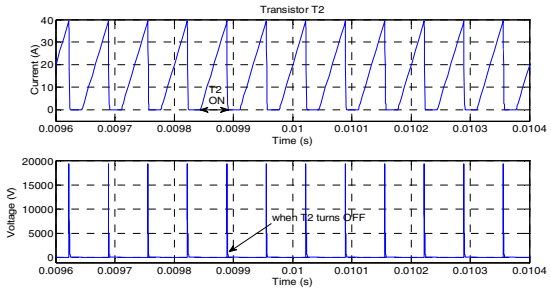


Fig. 18. T2 current and voltage waveforms during fault mode 6

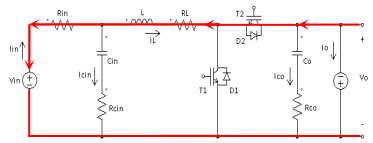


Fig. 19. Fault 7 operation mode

VI. CONCLUSION

This paper presents modeling, design and analysis of a half-bridge bidirectional DC/DC converter as a PEI between a HESS and the main DC bus in HEVs. The converter components are sized based on the design requirements of a full HEV. To verify the converter operation, the proposed design is simulated using Matlab/Simulink. Table V summarizes the converter simulation results under normal and faulty conditions for boost and buck operations. The effect of power switching device faults resulting from SC and OC diodes and transistors is analyzed. In summary, fault modes 1, 2, 3, 5, 6, and 7 can damage the power converter; whereas, OC transistor faults do not damage the power converter. When T2 is OC, the energy storage unit is directly to the dc-link; the PEI continues operation but not as a boost converter. When T1 is OC, the energy storage unit is completely disconnected from the dc-link; the converter behaves as if it is shut down. On the other hand, OC diode faults, result in high voltage spikes across the converter power switching components which could damage the power device. Whereas, SC diodes and transistors give rise to large bursts of current flowing through the converter components. In conclusion, the parameters measured for control purposes, such as the converter output voltage/current and the inductor voltage and current, can be used as key parameters in detecting and identifying the fault mode where techniques such as residual redundancy and higher-order moments are recommended with such types of faults.

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TABLE V. BIDIRECTIONAL DC/DC CONVERTER KEY PARAMETERS UNDER NORMAL AND FAULTY OPERATIONS

Operation Mode		I_{D1}	V_{D1}	I_{D2}	V_{D2}	I_{T1}	V_{T1}	I_{T2}	V_{T2}	I_L	V_L	*Output*
Boost	**Normal**	Off	Off	100A[a]	194V[a]	49A[a]	200V[a]	Off	Off	150V[c]	-1V[a]	288V[c]
	Fault 1	Off	Off	65A[a]	0V	1105A[a]	184V[a]	Off	Off	1230A[c]	-4[a]	184V[a]
	Fault 2	Off	Off	0	spikes	5A[a]	Spikes	Off	Off	5A[a]	spikes	0
	Fault 3	Off	Off	0	0	13.33kA[b]	0	Off	Off	13.33kA[b]	0.0667V[b]	0
	Fault 4	Off	Off	100A[c]	0.9V[c]	0	200V[c]	Off	Off	100A[c]	0.5V[c]	198V[c]
Buck	**Normal**	50A[a]	-200V[a]	off	off	off	Off	100A[a]	100V[a]	150A[c]	0.67V[a]	150A[c]
	Fault 5	-311.33kA[b]	0	off	off	off	Off	300kA[b]	V_{link}	-11.33kA[b]	0	0
	Fault 6	0	spikes	off	off	off	Off	27A[a]	Spikes	27A[a]	spikes	27A[a]
	Fault 7	0	- V_{link}	off	off	off	Off	8.67kA[b]	0	8.67kA[b]	V_{link}-V_{source}	8.67kA[b]
	Fault 8	0	-V_{source}	off	off	off	Off	0	V_{link}-V_{source}	0	0	0

[a.] average value [b.] constant value [c.] average value at steady state