Low Power Multiplier Architectures Using Vedic Mathematics in 45nm Technology for High Speed Computing

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Abstract— Speed and the overall performance of any digital signal processor are largely determined by the efficiency of the multiplier units present within. The use of Vedic mathematics has resulted in significant improvement in the performance of multiplier architectures used for high speed computing. This paper proposes 4-bit and 8-bit multiplier architectures based on Urdhva Tiryakbhyam sutra. These low power designs are realized in 45 nm CMOS Process technology using Cadence EDA tool.

Keywords— Vedic multiplier, Urdhva Tiryakbhyam, CMOS, High speed, Low power

I. INTRODUCTION

Real time digital signal processing today involves rigorous multiplication operations, which increases the computational complexity of modern day signal processors. The performance of such processors largely rests on the effectiveness of the multiplier units embedded within. A typical multiplier block comprises of a chain of AND gates to generate the partial product terms and an adder assembly to add them. The speed limitation associated with conventional multiplier architectures is largely due to the latency introduced by long adder tree structures. The power consumption of a multiplier unit is also a major design concern. Several research works have been reported over the years to optimize the performance of multiplier topologies. The basic approaches are to reduce the switching activity of the partial products [1], to reduce the number of nonzero partial product terms by effective encoding of the multiplier inputs and to realize a high speed adder tree for fast addition of the partial products. The Booth encoded multiplier topology [2, 3], Wallace tree based multiplier design [4-5] and compressor based multiplier architecture have provided noticeable performance enhancement over the conventional array multiplier. However the use of Vedic mathematics for multiplication [6-10] resulted in significant improvement in the overall speed and power consumption of a multiplier topology, due to the parallel computing approach.

The paper proposes low power multiplier architectures based on Vedic mathematics for high speed computing. The proposed 4-bit and 8-bit multiplier topologies based on the *Urdhva Tiryakbhyam* (vertically and crosswise) [11] sutra of Vedic mathematics are realized using 45nm CMOS process technology in Cadence EDA tool. A 5T AND gate design, based on pass transistor logic and transmission gate logic, has been used in this work for generation of partial products instead of the conventional 6T CMOS based design. The adder chains used in the multiplier units comprise of 14T full adders and 9T half adders optimized for low power and high speed arithmetic. The use of such modified topologies results in a smaller on chip silicon area requirement. The overall delay associated with the proposed architectures is also reduced as the number of transistors in the critical path is fewer, with the introduction of the new adder topologies. The performance analysis of the proposed designs is carried out for both schematic and layout stages with 1V voltage supply.

The rest of the paper is organised as follows. Section II provides a general overview of the Vedic mathematical approach utilised in the design. Section III gives a detailed discussion on the multiplier architecture along with a brief description of the various building blocks. The next section summarizes the performance evaluation and the result analysis. Section V concludes the paper.

II. URDHVA TIRYAKBHYAM (UT) SUTRA

Vedic mathematical approaches provide effective computing methodologies for high speed arithmetic. The *Urdhva Tiryakbhyam* (UT) sutra described in Vedas is an effective way for realizing fast multiplication operations. The use of UT sutra for multiplication operation reduces the latency of a multiplier unit by introducing parallel computing of partial products.

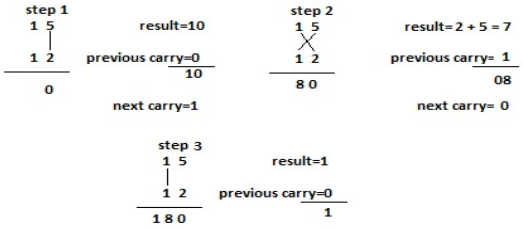

Fig. 1 UT based multiplication for 2 digit decimal numbers

The sutra literally means vertically and crosswise, which is illustrated in the Fig. 1 for a two digit decimal multiplication. The UT sutra is conventionally used for multiplication in decimal number domain. However it can be extended to execute binary number arithmetic. The line diagram of binary multiplication using UT method for 2-bit, 3-bit and 4-bit numbers is shown in Fig. 2.

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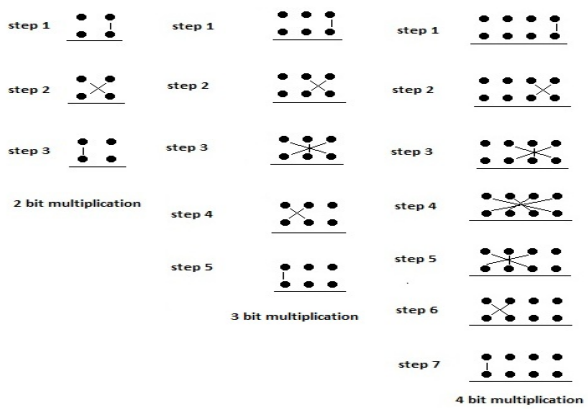

Fig. 2 Line diagram for binary multiplication using UT sutra

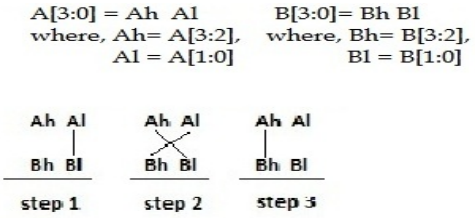

Fig. 3 4-bit multiplication using 2-bit UT multiplication analogy

The partial product generation as indicated by the vertical and crosswise lines in the figure is primarily an AND operation For the 2-bit multiplication of two arbitrary inputs A [1:0] and B[1:0] the following expressions are obtained.

$$P_0 = B_0A_0 \quad (1)$$
$$C_1P_1 = B_0A_1 + B_1A_0 \quad (2)$$
$$C_2P_2 = C_1 + B_1A_1 \quad (3)$$

Where, B_iA_j represents the partial product terms for corresponding bit positions *i* and *j* of the operands, C_1 and C_2 are the carries generated from partial product addition and $C_2P_2P_1P_0$ is the result of the multiplication. The 4-bit multiplication, as shown in the line diagram of Fig. 2, can also be carried out by using 2-bit Vedic multipliers [10]. Any 4-bit binary number A can be represented as A_hA_l where A_h is the most significant 2 bit positions and A_l is the least significant 2 bit positions. A similar analogy is extended to the number B which is represented as B_hB_l. Now the multiplication of A and B is identical to a 2-bit Vedic multiplication approach as indicated in Fig. 3. Following the same analogy, two 8-bit binary numbers A and B, represented as A_hA_l and B_hB_l respectively, where A_h and B_h are the higher nibbles and A_l and B_l are the lower nibbles, can be multiplied using 4-bit multiplier blocks. The corresponding line diagram is provided in Fig. 11.

III. MULTIPLIER ARCHITECTURE

The multiplier architectures proposed in this paper are based on UT sutra of Vedic mathematics. The partial product generation in all the designs is realized by 5T pass transistor and transmission gate based AND gates which is described shortly. The use of such a modified AND gate design ensures a significant reduction in the overall on-chip area occupied by the multiplier. As the number of AND gates used for partial product generation increases quadratically with the word length, the use of this modified design plays a greater role for higher order multipliers (32-bit, 64-bit *etc.*) The adder chain, for the proposed multiplier architectures, incorporates new full adder and half adder topologies that are optimized for low power, high speed and full swing applications. The overall improvement in delay characteristics of the multipliers is attributed to the use of these new adder units which addresses the main performance bottleneck associated with the conventional designs i.e. the latency introduced by the adder assembly. The adder architectures are also discussed below.

A. AND Gate

A 5T based AND gate, given in Fig. 4, is utilized in this paper for the partial product generation. The AND gate utilises pass transistor logic and transmission gate based logic [12]. It is basically a multiplexer based approach which implies the output A AND B, with any arbitrary operands A and B, is same as B for A being equal to logic 1 and is grounded for A being logic 0. The design makes use of fewer (i.e. 5) transistors as compared to the conventional 6T based CMOS design and hence results in a reduction of the overall on chip area requirement of the complete multiplier architecture. An 8-bit binary multiplier incorporates 64 AND gates for partial product generation and thus the use of the new AND gate topology brings down the number of transistors by 64 per each multiplier unit. However, the use of such designs does not affect the delay characteristics significantly as the partial product generation is performed parallelly.

B. Half Adder

The half adder block used in this paper is a 9T design that ensures high speed, low power and full swing arithmetic. As shown in Fig. 5, the topology uses a 5T AND gate for carry generation while the sum generation unit comprises of a 4T XOR gate. The smaller transistor count ensures a compact design and smaller power dissipation along with an improved delay characteristics. The full swing output logic realization enables the topologies to be used in cascaded arrangements efficiently without the need of any additional swing restoring buffer units.

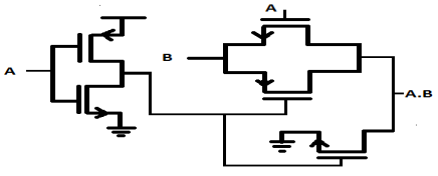

Fig. 4 Modified AND gate design

C. *Full Adder*

The speed of a multiplier block is essentially limited due to the latency introduced by the adder assembly incorporated in it for adding the partial products. The use of conventional adder architectures for realizing these long adder chains would not suffice the need of high speed computing of the modern day signal processors because of the large propagation delay and high power consumption associated with them [13]. Hence there is a need to use new full adder architectures that could ensure high speed and low power arithmetic [14-16]. The 14T topology [17], presented in Fig. 6,is basically a multiplexer based architecture that ensures full swing output voltages at both sum and carry-out terminals. The compact design and smaller transistor count associated with this topology provides significant improvement in the performance of the adder chains embedded in the multiplier. The inherent full swing based adder architecture also eliminates the need of additional swing restoring buffer units and is suitable for cascaded arrangements (as carry save adder blocks as used in this work). The low power dissipation associated with the adder topology essentially reduces the overall power consumption of the multiplier unit and ensures a power efficient high speed computing.

D. *2-bit Vedic Multiplier Architecture*

The UT based 2-bit Vedic multiplier presented in this work comprises of four AND gates for partial product generation and two half adders to realize the required addition process. The overall propagation delay associated with the design can be estimated as one AND gate delay (because all the AND gates are used for a parallel computation of the partial products) plus two half adder delays. Because of the high speed adder architectures and the modified AND gate topology, the overall performance of the multiplier is improved significantly. The topology, shown in Fig. 7, is a 38T design.

E. *4-bit Vedic Multiplier Architecture:*

The Vedic mathematics based 4-bit binary multiplier can be realized using the Urdhva Tiryakbhyam sutra as explained in the line diagram of Fig. 2. All the partial products are generated in parallel using a chain of AND gates. The addition of partial products can be accomplished by implementing several carry save adder arrangements and a final vector merging adder. The corresponding topology is given in Fig. 8. The use of half adder units (instead of full adder blocks) in the first bit addition stage of the carry save adder arrangement and also in the final vector merging adder results in some reduction in the overall layout area and the power consumption. The 4-bit binary multiplier can also be realized using 2-bit multiplier analogy, as illustrated in Fig. 3. The paper proposes a novel architecture to implement such a design.

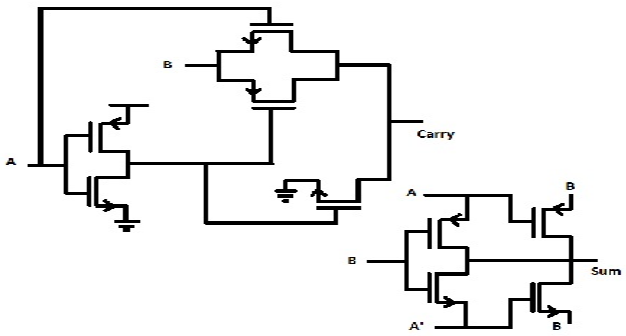

Fig. 5 Half Adder design

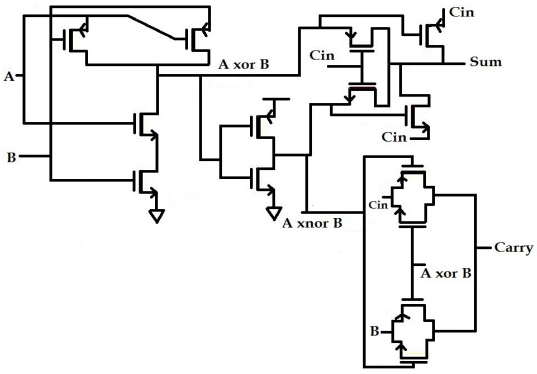

Fig. 6 Full Adder design

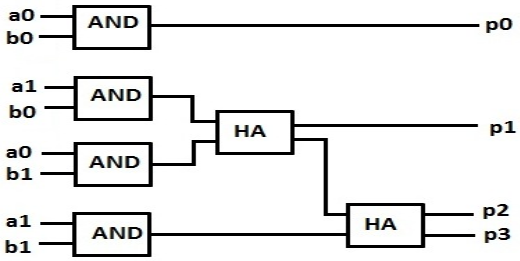

Fig. 7 UT based 2-bit Multiplier Architecture

This UT based architecture, as shown in Fig. 9, incorporates four 2×2 Vedic multiplier units which ensure a parallel computing approach. Several adder blocks are incorporated in the proposed architecture for addition of the intermediate results generated from the 2-bit multiplier blocks. Two 4-bit carry save adder arrangements and one 4-bit vector merging adder are used in this architecture. Previously reported works of similar nature have utilised greater number of adder blocks as compared to the proposed work for realizing an equivalent multiplication task. Hence by reducing the hardware requirement, the proposed topology ensures an improved performance in terms of the compactness of the design. The use of high speed and power efficient adder units also provides a significant improvement in the propagation delay and the power dissipation. The multiplier topology introduces differential delay paths for different bits of the output. The least significant two bits of the output are

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stable after one 2-bit Vedic multiplier delay whereas the most significant bit of the result is obtained after a larger delay. The exact propagation delay associated with the MSB can be modelled as one 2-bit multiplier delay plus two full adder delays (due to the Carry Save Adder arrangement) plus the delay introduced by the 4-bit ripple carry adder stage. The ripple carry adder is realized with an assembly of three full adders (14T) and one half adder unit (9T), and hence accounts for a 51 transistor design. Because of the dissimilar delay profile, the overall speed of the topology is approximated from the maximum delay path associated with it, which is the delay from any of the input bits to the most significant bit of the product. The UT based multiplication approach can also be utilized to implement four bit signed number arithmetic. In a signed number representation scheme using four bit numbers, the most significant bit (MSB) usually represent the signed bit, whereas the lower three bits represent the magnitude of the number [12]. In a 4-bit signed multiplication, the most significant bits of the two operands can be passed through a XOR logic block to determine the sign of the result. The rest of the three bits can be multiplied as indicated in the line diagram of Fig. 2 using the UT sutra to determine the signed magnitude of the result. The corresponding architecture is presented in Fig. 10. The cliché in this kind of a system is the sign bit or the MSB of the result appears earlier, as compared to the other bit positions, because of the dissimilar delay paths. If required, this issue can be addressed by implementing desired buffer arrangements in the MSB generation unit. However such an arrangement is not included in the proposed design.

F. 8-bit Vedic Multiplier Architecture

The UT based 8-bit Vedic multiplier presented in this work is based on the analogy given in Fig. 11. Four 4×4 multiplier blocks and several adder units can be utilised to realize the proposed topology. The design, presented in Fig. 12, is a carry save architecture based on the UT sutra for improvement in overall speed of the topology. In the figure two 8-bit inputs A [7:0] and B [7:0] are multiplied to generate a 16-bit output P [15-0]. The adder blocks used in the design do not introduce large latency as most of them are used in a carry save arrangement. The overall propagation delay of the architecture can be estimated as one 4×4 multiplier delay, three full adder delays (due to the 8-bit carry save adder arrangements) and the delay introduced by the 8-bit ripple carry adder in the final addition stage. The transistor count associated with this design is in the higher side; however the hardware complexity is justified as it results in an improved performance. The 4-bit multipliers used in the proposed architecture are UT based 4-bit Vedic multipliers as shown in Fig. 9. It can be seen in Fig. 12 that some of the inputs to the carry save adder blocks are accompanied by zero padding. This is done to ensure uniform bit-lengths for all the inputs to a particular carry save adder stage.

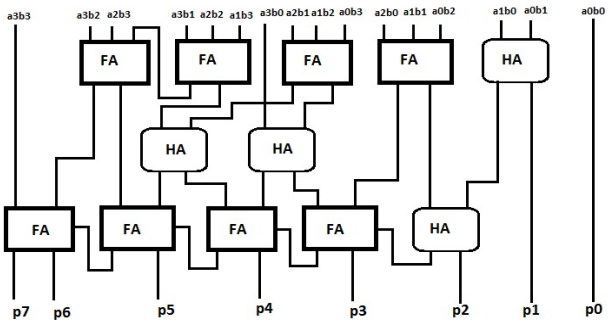

Fig. 8 4-bit multiplier design1

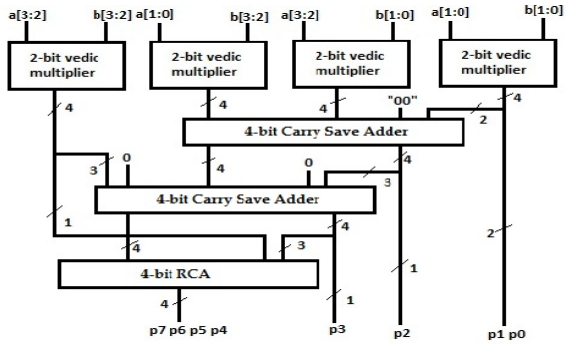

Fig. 9 4-bit multiplier design2

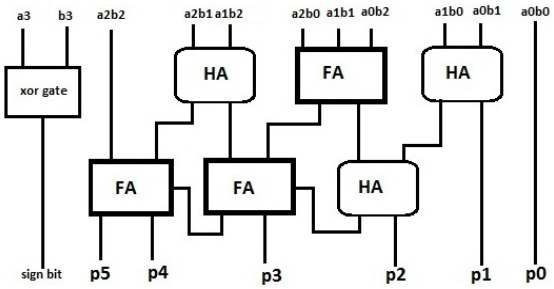

Fig. 10 4-bit signed multiplier

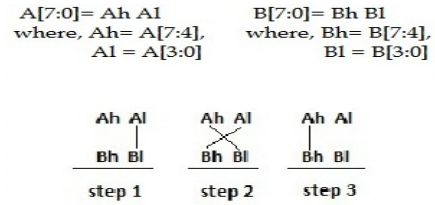

Fig. 11 8-bit multiplication using 2-bit UT multiplication analogy

IV. PERFORMANCE ANALYSIS

Performance analysis of the multiplier topologies presented in this paper is performed using the Cadence EDA tool, in 45nm CMOS process technology. The schematics and the av-extracted (layout with parasitics) views of the topologies are subjected to several test input combinations at a power supply of 1 volt, to analyse the power consumption and overall operating speed.

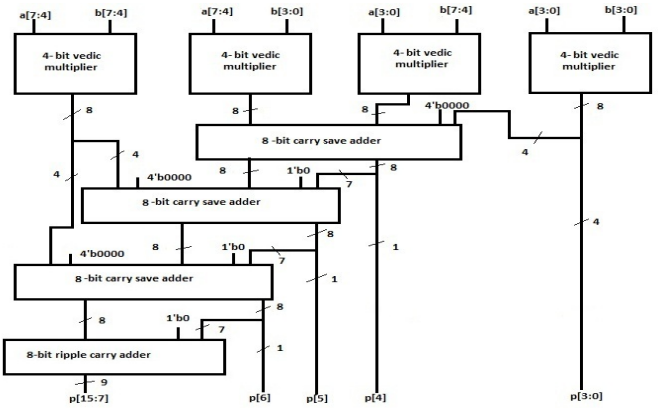

Fig. 12 8-bit multiplier design based on UT sutra

The results obtained are compared with existing architectures to approximate the effectiveness of the proposed architectures. The topologies are also subjected to corner analysis to validate their robustness. The results are tabulated in TABLE I-IV. TABLE I represents the transistor count associated with the topologies along with the total on chip silicon area occupied by the multiplier architectures. The use of modified designs for the AND gate ,the half adder and the full adder units accounts for the overall compactness of the multiplier architectures as these topologies utilize less number of transistors as opposed to the conventional designs. As compared to the CMOS based AND gate design, the modified topology used in this paper suffers from an irregular layout issue. Though it does not provide any significant advantage over the CMOS based design with respect to propagation delay because of the parallel computing of partial products, this 5T topology is preferred to reduce the layout area. TABLE II enlists the propagation delays and power consumptions associated with the proposed designs, both for the schematic and av-extracted cellviews. Among the two 4-bit fixed point multiplier designs, design-1 happens to be more efficient as far as the propagation delay is considered.

TABLE I. Transistor Count and Layout Area

Name of the topology	**Transistor Count**	**Layout Area (in μm^2)**
4-bit Vedic Multiplier-1	228	341.23
4-bit Vedic Multiplier-2	320	549.31
4-bit Signed Multiplier	120	221.49
8-bit Vedic Multiplier	1648	5080.38

However design-2 displays significant improvement in power consumption. A comparative analysis of propagation delays of different existing 8-bit multiplier architectures reported in the literature with the proposed architecture is presented in TABLE III. The comparison indicates that with respect to the different existing multiplier algorithms and architectures, the proposed design offers improved speed at considerably smaller power consumption with 1 volt power supply. The improved performance can be accounted to the new UT based architecture as well as the use of low power and high speed half adder and full adder units. However, further improvement in the proposed architectures is essential to achieve better delay characteristics as reported in [18]. The proposed 4-bit and 8-bit multiplier designs are subjected to corner analysis at the five possible process corners. A process corner represents a three or six sigma variation from nominal doping concentrations (and other such fabrication parameters) that allow a designer to test any design against various adverse fabrication conditions in order to verify the robustness. In a convention, three process corners are said to exist, namely typical, fast and slow, where the first one corresponds to nominal fabrication conditions, while the other two correspond to conditions with higher and lower carrier mobility (with respect to nominal value) respectively.

TABLE II. Propagation Delay and Power Consumption of different multiplier topologies

Name of the topology	**Propagation Delay (in ns)**		**Power Consumption (in µw)**	
	Schematic	***Av-Extracted***	***Schematic***	***Av-Extracted***
4-bit vedic Multiplier-1	0.138	0.349	0.955	2.956
4-bit vedic Multiplier2	0.268	0.754	0.842	2.550
4-bit Signed Multiplier	0.127	0.382	0.491	1.606
8-bit vedic Multiplier	0.635	3.479	7.460	26.76

TABLE III. Performance Comparison

Name of the topology	**Power Supply / Technology**	**Propagation Delay (in ns)**	**Power Consumption**
Proposed 8-bit multiplier	1v (45 nm)	0.635	7.46 µw
[10]	-	14.41	-
[18]	180 nm	0.135	1.414 mw
[19]	180 nm	0.95	16 mw
[20]	350 nm	4.53	4.86 mw
[6]	-	13.07	-
[7]	-	7.72	3.67 mw
[8]	-	6.781	64.21 mw
[9]	-	15.418	-

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Thus, in general, five such process corners are possible, notably ff (fast-fast), fs (fast-slow), sf (slow-fast), ss (slow-slow) and tt (typical-typical; same as normal process corner) where the first letter in the naming convention indicates the NMOS condition and the second letter corresponds to the PMOS condition The results of the pre-layout corner analysis are presented in TABLE IV.

TABLE IV. Pre-layout Corner Analysis

Topology	Parameter	ff	fs	sf	ss	tt
4-bit Vedic multiplier1	Propagation delay (in ns)	0.10	0.13	0.15	0.20	0.14
	Power consumption (in µw)	1.01	1.04	0.94	0.92	0.95
4-bit Vedic multiplier2	Propagation delay (in ns)	0.18	0.31	0.24	0.53	0.27
	Power consumption (in µw)	0.93	1.07	0.82	0.79	0.84
4-bit signed multiplier	Propagation delay (in ns)	0.10	0.13	0.14	0.17	0.12
	Power consumption (in µw)	0.52	0.57	0.47	0.47	0.49
8-bit Vedic multiplier	Propagation delay (in ns)	0.41	0.68	0.77	1.18	0.64
	Power consumption (in µw)	7.81	11.6	6.53	6.79	7.46

V. CONCLUSION

The paper presents new topologies for 4-bit and 8-bit multipliers based on UT sutra of Vedic mathematics. The topologies are realized in 45 nm CMOS process technology in Cadence EDA tool and the performance analysis is performed using several test inputs with a power supply of 1 volt, both for the pre layout and post layout stages. A process corner analysis of the proposed designs is presented at the five different process corners to validate the robustness of the architectures. The multiplier designs proposed in this paper demonstrate noticeable improvement in propagation speed and power consumption and the improvement in performance is achieved due to the new UT based architecture with fewer number of adder units (reduced data path). The low power and high speed adder blocks used in the designs ensure power efficient and high speed computing. A reduction in total on chip silicon area is also achieved by implementing the partial product generation unit with the help of 5T AND gates.

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