High-Speed, Modified, Bulk stimulated, Ultra-Low-Voltage, Domino Inverter

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***Abstract*— In this paper, a new Ultra low voltage (ULV) logic circuit based on the floating gate structure is presented. In this technique we utilized the bulks of the transistors to speed up the circuit. Using the proposed method, the speed of the circuit enhances by connecting the bulks of the evaluating and precharge devices to the clock, power supply (VDD) and input signals. The simulation results for the designed ULV logic in a typical *90nm* CMOS technology show more than 40% delay reduction. Higher speed in the lower supply voltages and robustness against process variations are the main advantages of the proposed approach in comparison to the previously reported FGULV and other ULV methods.**

***Index Terms*— Ultra Low Voltage (ULV), Floating Gate; Speed, Bulk**

I. INTRODUCTION

As the semiconductor industry grows, the demand for Ultra Low Voltage (ULV) circuits is increasing. Power reduction techniques are proposed to improve the battery life of the applications such as implantable biomedical systems laptop computers, personal digital assistants, and portable communication devices. One of the most important techniques to lower power consumption is supply voltage scaling. By scaling the supply voltage, the dynamic power is reduced significantly. For wireless sensor network applications, due to lower frequency rate, the supply voltage may be reduced below the threshold voltage. This operation is referred as sub-threshold design that uses the sub-threshold current as drive current to evaluate the inputs [1, 2]. Lowering the supply voltage reduces the sub-threshold current, exponentially. The optimal supply voltage for CMOS logic in terms of EDP (Energy delay product) is close to the threshold voltage of the nMOS transistor Vtn for a specific process, assuming that the threshold voltage of the pMOS transistor Vtp is approximately equal to Vtn [3]. Low voltage digital CMOS becomes more and more attractive, due to the general advances in process technology and due to the low power applications. The aggressive scaling of device dimensions and supply voltage in order to achieve greater transistor density and low power consumption results in degradation in the speed of the logic circuits due to reduced effective input voltage on gate source of the transistors. On one hand, the ever increasing market segment of portable electronic devices demands the availability of low-power building blocks that enable the implementation of long-lasting battery-operated systems. On the other hand, the general trend of increasing operating frequencies and circuit complexity, in order to cope with the throughput needed in the modern high-performance processing applications, requires the design of very high-speed circuits. Several techniques for high speed and low voltage digital CMOS circuits have been presented in [4]. Floating-Gate (FG) gates have been proposed for ULV domino logic [3]. FG logic implemented in a modern CMOS process requires frequent initialization to avoid significant leakage. By using input floating capacitances to the transistor gate terminals, the semi-floating-gate (SFG) nodes can have a different DC level than provided by the supply voltage headroom [5]. There are several approaches for both analog and digital applications using FG CMOS logic proposed in [6-9]. The gates proposed in this paper are influenced by the ULV non-volatile FG circuits [10]. In this paper a new bulk stimulation technique is utilized to speed up the domino logic structures, by reducing the threshold voltage of transistors. Different topologies are studied and simulation results are reported. The proposed technique is applicable to other floating gate ULV (FGULV) domino logic structures like carry generators [11], NAND and NOR gates [12], and FGULV Flip-Flops [13].

This paper is organized as follows: in Sect.2, the simple domino FGULV inverter and also the proposed domino FGULV inverter circuit are presented and the circuit specifications are compared for the different topologies; in Sect.3, the simulation results for the different FGULV inverter

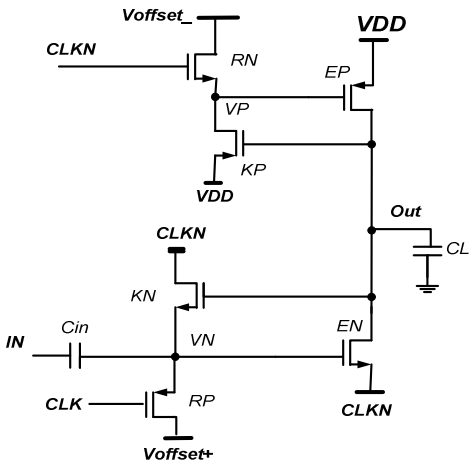

Fig. 1 Simple FGULV Domino inverter. (Precharg to 1).

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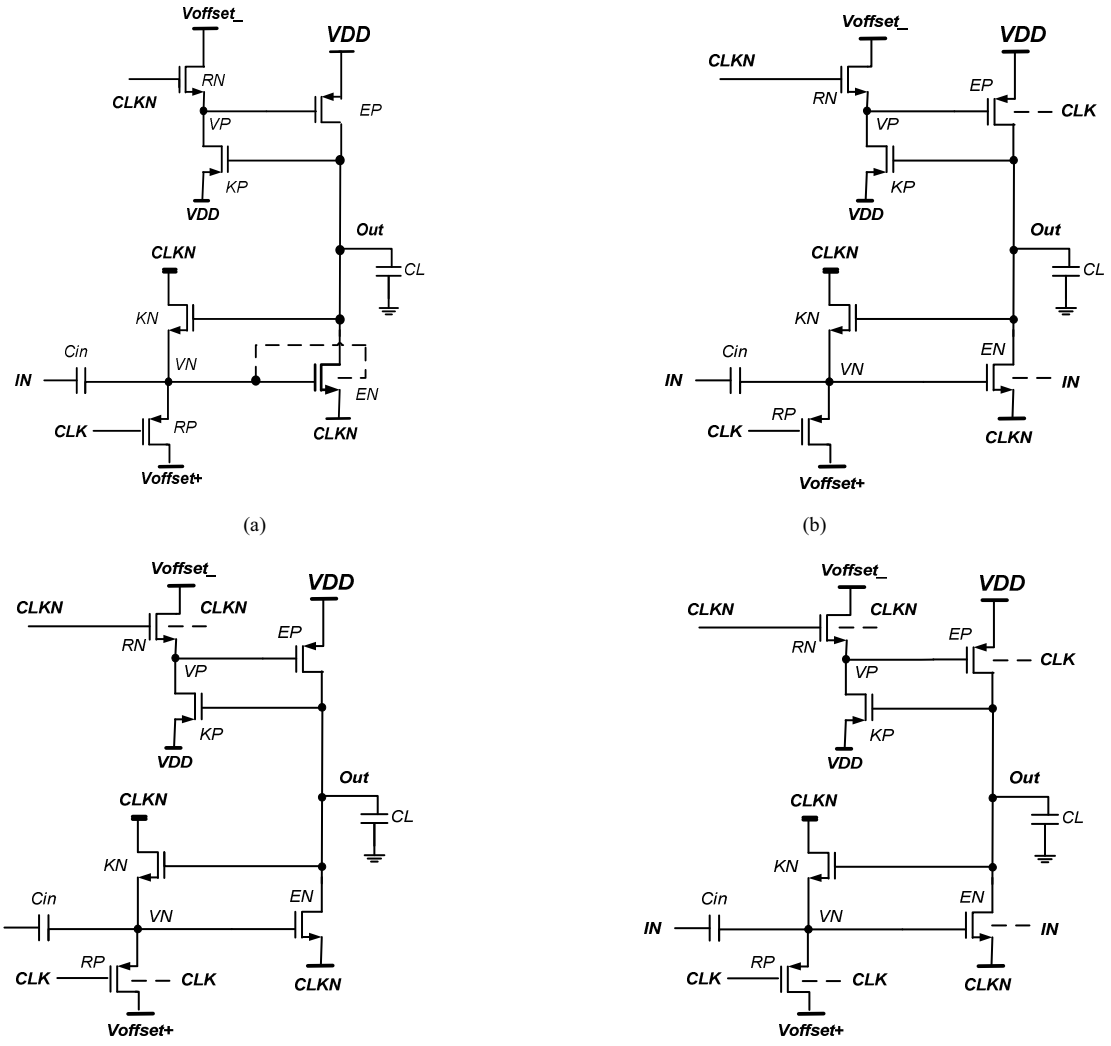

Fig. 2. Different domino FGULV inverters with bulk stimulating technique (a) Bulk of EN is connected to floating gate node (VN) (b) Bulk of EN is connected to the Input and the bulk of the EP devices is connected to the CLK signal. (c) Bulk of the RN is connected to the CLKN and the bulk of the RP is connected to CLK (d) The bulk of the precharge and evaluate devices are manipulated.

circuits are given, and compared with the simple FGULV inverter circuit; finally Sect.4 concludes the paper.

II. DOMINO FGULV LOGIC

The ULV domino gate presented in this paper is related to the FGULV domino logic style presented in [11-13]. The main purpose of the FGULV domino logic style is to increase the current level for the transistors at low supply voltages without increasing the transistor widths. We may increase the current level compared to complementary static CMOS using different initialization voltages to the gates and applying capacitive inputs. The extra load represented by the input capacitors (Cin) is less than the extra load given by increased transistor widths. The capacitive inputs lower the delay through increased transconductance while increased transistor widths only reduce the parasitic delay. The proposed logic style may be used in the critical high speed and low voltage systems together with the conventional CMOS logic. In these topologies Voffset+ pins are connected to the VDD and Voffset- pins are connected to the GND and CLKN signal is the inversion of the CLK signal.

A. Simple FGULV inverter

The High-speed N-type FGULV domino inverter (precharge to 1) presented in [11], is shown in Figure 1. The clock signals CLK and CLKN are used both as control signals for the recharge transistors RP and RN, and as reference signals for NMOS evaluation transistor EN.

When CLK switches from 1 to 0, the circuit becomes in the precharge/recharge phase. During this phase, RP turns on and

recharges the gate of EN transistor to 1. Meanwhile CKN switches from 0 to 1 which turns on RN and recharges the gate of EP to 0. Thus EP turns on and precharge the output node Vout to VDD. The keeper transistors, KN and KP, are inactive during this phase as the output node is precharged to1.

In the evaluation phase, clock signals CLK and CKN switch from 0 to 1 and 1 to 0 respectively. Both recharge transistors RP and RN switch off which make the charge on the gate terminals Vp and Vn floating. The output node Vout remains high (VDD) until a rising transition occurs at the input signal. The input signal Vin must be monotonically rising to ensure the correct operation for the N type domino inverter. This can only be satisfied if the input signal Vin is low at the beginning of the evaluation phase, and if Vin only makes a single transition from 0 to 1 in the evaluation phase. When this transition happens (Vin goes from 0 to 1), in the ideal case, the voltage of semi-floating gate (VN) increases up to 2VDD and this increases the current of EN in the evaluating phase and speed up the evaluation process. KN turns on when the output node gets a negative transition in the evaluation phase. This partially turns off the evaluation transistor (EN) and let the output node swings fully to GND. This helps to reduce the static current which directly impacts on the noise margin and the power consumption of the proposed logic. As it mentioned in the recent research reports, the FGULV logic demonstrates significant speed improvements in comparison to conventional static CMOS logic [8-15].

B. Proposed domino FGULV inverters

The proposed High-speed N-type FGULV domino inverters (precharge to 1)], are shown in Figure 2. In these topologies Voffset+ pins are connected to VDD and Voffset- pins are connected to GND. Body biasing technique is utilized in the different logic structures to reduce the threshold voltages of the devices. This threshold reduction helps the logic circuits to operate in the higher speed, especially in the ultra low voltage circuits (eg. [14]. In the Figure 2 (a), the bulk pin of evaluating device (EN) is connected to semi-floating gate node (VN). In this topology the threshold voltage of evaluating devices are reduced in the evaluating phase and this increase the ON current of the evaluating devices in the evaluating phase. However in this topology parasitic capacitance of VN node is increases and this causes to have larger parasitic capacitance at VN node. With larger parasitic capacitance at VN node, small portion of the input signal (IN) drops in VN node and this can reduce the speed of logic in the evaluating mode. So an optimum size should be chosen for devices and input capacitor (Cin) in order to maximize the speed.

Another way to manipulate the bulks of the devices in the FGULV is shown in Figure 2 (b). In this topology the bulk pin of evaluating device (EN) is connected to input signal and the bulk of EP device is connected to CLK signal. As mentioned before connecting the bulk of an NMOS device to VDD, reduces the threshold voltage of that device and increases the current of that device and finally reduces the delay in evaluating phase. The bulk of EP is connected to CLK signal. In the precharge phase, when EP is charging the output node, connecting the bulk of this device to the minimum possible

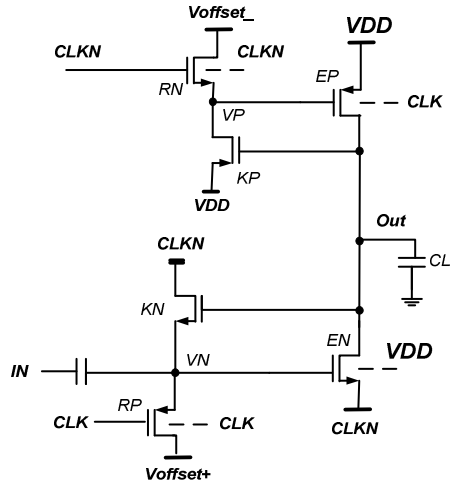

Fig 3. the Bulk of the Precharge devices are stimulated with the clock and the bulk of EN is connected to VDD.

voltage in the circuit (GND), reduces the threshold voltage of that device and this speed up the precharge process as well. In the evaluating phase, since CLK signal is high (VDD), the bulk of EP is connects to VDD and this device has bigger threshold voltage and less leakage current as well. In the topology shown in Figure 2(c), the bulks of RN and RP devices are manipulated to speed up the precharge process. Bulk of RP is connected to CLK signal. This connection reduces the threshold voltage of this device in the precharge phase and speeds up the precharge process for VN node. In the evaluating phase (CLK=1), in order to minimize the leakage current, the voltage of the bulk of this device (RP) goes high and it doesn't have small threshold voltage anymore. The bulk of RN is connected to CLKN signal. This connection reduces the threshold voltage of this device in the precharge phase and speeds up the precharge process for VP node. In the evaluating phase (CLK=1), in order to minimize the leakage current, the voltage of the bulk of this device (RN) goes low and so it will have the normal threshold voltage.

In the topology shown in Figure 2(d), the bulks of RN and RP devices are manipulated by clock signal, to speed up the precharge process. Also in this topology the bulk of the EN is connected to input signal to increase the current and speed of the evaluating process. The effectiveness of this structure should be evaluated in a chain of different inverters, since the parasitic bulk capacitance of the evaluating devices are added to the overall parasitic capacitance of the output node of the previous inverter, and this can reduce the overall speed of the chain. In the topology shown in Fig.3, the bulk of EN device is connected to VDD, and also the bulks of RN, EP and RP devices are manipulated by the clock signals.

III. Simulation Results

In this section, the simulation results for the different FGULVs are presented and compared. The simulations for the designed FGULV logic inverters are done using cadence software in a typical *90nm* CMOS technology. Low threshold voltage devices are chosen to speed up the circuit. To verify the effect of the bulk stimulation method on the performance of the

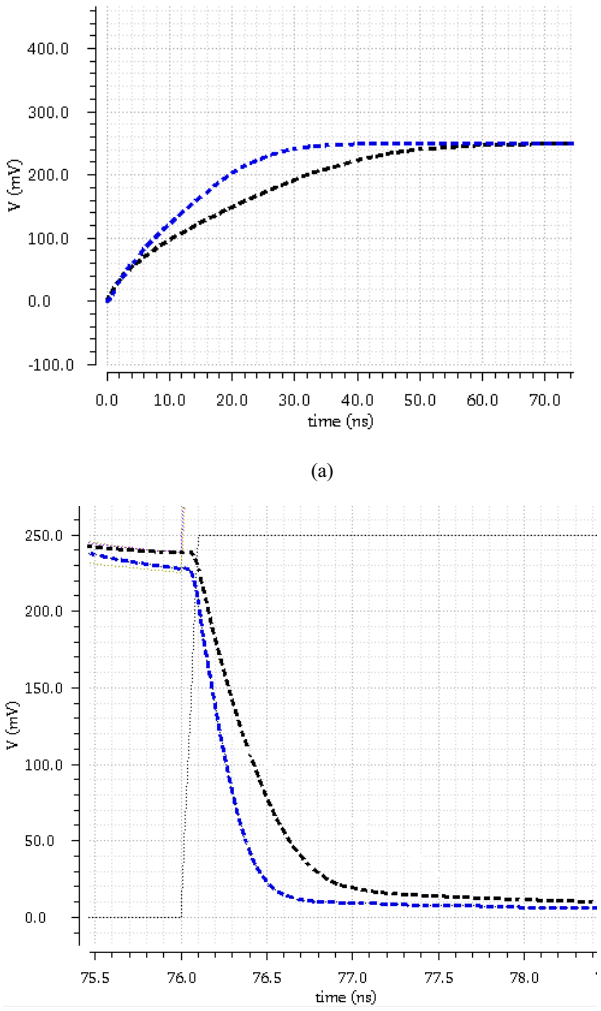

Fig 4. (a) The voltage of VN node in Precharge phase. (Blue is for proposed bulk stimulated precharge devices and black is for simple FGULV). (b) The voltage of output node in the evaluating phase. (Blue is for proposed bulk stimulated evaluating devices (EN) and black is for simple FGULV)

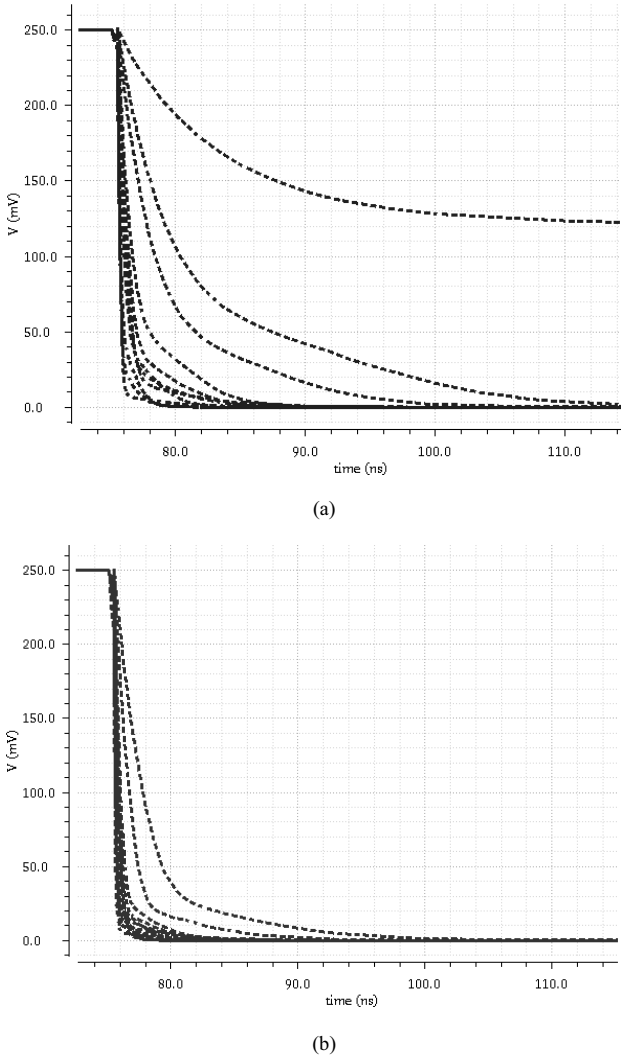

Fig 5. Monto- Carlo simulation results when VDD is 250mV. (a) The Output voltage in the evaluation phase for simple FGULV inverter shown in Fig.1. (b) The Output voltage in the evaluation phase for FGULV inverter shown in Fig.3.

FGULV, different FGULVs, shown in Fig.1, Fig.2 and Fig.3 are designed in the same size and power supply, and finally the characteristics are compared. In the all designed circuits, a 2fF capacitor is chosen for input capacitor (Cin). Simulation result shows that this size is optimum capacitor size for maximum speed, when the minimum size devices are used for inverter. Smaller capacitor (eg. 1fF) causes a voltage swing reduction from input signal to the semi-floating gate (VN) and this reduces the speed. Larger input capacitors also reduce the overall speed of the domino logic, since this capacitors adds to the output capacitance of the previous (precharge to 0) inverter. All the topologies shown in the Fig.2 and Fig.3 have been designed in a typical 90nm CMOS process with the same capacitor load. Simulation results show that for the evaluating phase, structure presented in the Fig. 3 has maximum speed. Fig.4 shows the transient simulations results of the designed

FGULV domino logic inverters in this paper (shown in Fig. 3) with 250mV power supply. As shown in Fig.4, the FGULV domino logic presented in this paper, achieve higher speed both in the precharge and evaluating phase. The proposed circuits are simulated in the different power supplies. Simulation results show that the proposed circuits are operating properly with power supplies down to 100 mV. In those low power supplies, the speed reduces significantly, structures become more sensitive to process variations and overall performance of the structure reduces. However, as mentioned in the previously reported papers (e.g. [8-13]), FGULV inverter is much faster and more robust than conventional static CMOS logic inverter. For supply voltages in the region from 200mV to 400mV, the delay of the simple FGULV inverter, reduces more than 96% comparing to the delay of the standard static CMOS inverter in the same device size [9]. Fig. 5 shows the Monte-Carlo simulation results for both simple and proposed FGULV.

Monte-Carlo simulations show that the proposed FGULVs are more robust than simple FGULV against process variations. Also simulation results shows better noise margin for the proposed FGULV. The simulation results for the proposed FGULV logics in the different power supply voltages shows significant speed enhancement for the both precharge and evaluating phases.

IV. Conclusion

In this paper, new inverters based on the FGULV domino logic structure are presented which uses bulk pins of the different devices in the original FGULV domino logic inverter structure to speed up the circuits. By manipulating the bulk voltages of the transistors, in the different topologies, the threshold voltages of these devices are reduced to speed up the circuits. Using the presented method, delay of the FGULV Domino logic inverter is reduced more than 40% in the both precharge and evaluating phases. Different topologies for the proposed technique are presented and advantages and disadvantages of the designs are studied.

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