Energy and Area Efficient Three-Input XOR/XNORS With Systematic Cell Design Methodology
Tooraj Nikoubin, Mahdieh Grailoo, and Changzhi Li

Abstract—In this brief, we propose three efficient three-input XOR/XNOR circuits as the most significant blocks of digital systems with a new systematic cell design methodology (SCDM) in hybrid-CMOS logic style. SCDM, which is an extension of CDM, plays the essential role in designing efficient circuits. At first, it is deliberately given priority to general design goals in a base structure of circuits. This structure is generated systematically by employing binary decision diagram. After that, concerning high flexibility in design targets, SCDM aims to specific ones in the remaining three steps, which are wise selections of basic cells and amend mechanisms, as well as transistor sizing. In the end, the resultant three-input XOR/XNORs enjoy full swing and fairly balanced outputs. They perform well with supply voltage scaling, and their critical path contains only two transistors. They also outperform their counterparts exhibiting 27%–77% reduction in average energy-delay product in HSPICE simulation based on TSMC 0.13-µm technology. The symmetric schematic topologies significantly simplify and minimize the layout, as 26%–32% improvement in area is demonstrated.

Index Terms—Binary decision diagram applications, energy efficiency, hybrid-CMOS logic style, systematic design methodology, three-input XOR/XNOR circuits.

I. INTRODUCTION

With the rapid growth of portable electronic devices, it is becoming a critical challenge to design low-power, high-speed (LPHS) circuits that occupy small chip areas. We see many published papers that compete in designing better circuits [1]–[6]. Such studies mostly rely on creative design ideas but do not follow a systematic approach. As a consequence, most of them suffer from some different disadvantages [2].

1) They are implemented with logic styles that have an incomplete voltage swing in some internal nodes, which leads to static power dissipation.

2) Most of them suffer from severe output signal degradation and cannot sustain low-voltage operation.

3) They predominantly have dynamic power consumption for nonbalanced propagation delay inside and outside circuits, which results in glitches at the outputs.

Therefore, a well-organized design methodology can be regarded as a strong solution for the challenge. It is not try-and-error-driven, which means that it systematically and deliberately aims to the design goals. It also picks circuit components wisely and does not postpone the determination of the circuit characteristics after simulation. Cell design methodology (CDM) has been presented to design some limited functions, such as two-input XOR/XNOR and carry–inversecarry in the hybrid-CMOS style [7]–[9]. The predominant results persuade us to improve CDM through two stages: 1) generating more complex functions and 2) rectifying some remaining flaws. The flaws in previously published CDM include containing some manual steps in the design flow and generating a large number of designs in which the predominant ones would be determined after the completion of simulations. Therefore, in the first stage, a three-input XOR/XNOR as one of the most complex and all-purpose three-input basic gates in arithmetic circuits [10] has been chosen. If the efficiency of the circuits is confirmed in such a competitive environment, it can show the strength of the methodology. In the second stage, CDM is matured as systematic CDM (SCDM) in designing the three-input XOR/XNORS for the first time. It systematically generates elementary basic cell (EBC) using binary decision diagram (BDD), and wisely chooses circuit components based on a specific target. This takes place when the mentioned features are not considered in the CDM. Therefore, after the systematic generation, the SCDM considers circuit optimization based on our target in three steps: 1) wise selection of the basic cell; 2) wise selection of the amend mechanisms; and 3) transistor sizing. It should be noted that BDD can be utilized for EBC generation of other three-input functions. We consider the power-delay product (PDP) as the design target. It stands as a fair performance metric, precisely involving portable electronic system targets. The motivation to use this methodology is the presence of some unique features and the ability to produce some efficient circuits that enjoy all these advantages.

1) The SCDM divides a circuit structure into a main structure and optimization-correction mechanisms. In the main structure, it considers features including the least number of transistors in critical path, fairly balanced outputs, being power-ground-free, and symmetry. The mechanisms have the duty of completing the functionality of the circuits, avoiding any degradation on the output voltage, and increasing the driving capability.

2) The least number of transistors in critical path increases the chances of the circuit to have better characteristics, as experimental results have shown an average saving of 10%–50% and 27%–77% in terms of delay and Energy-Delay Product (EDP), respectively.

3) The dynamic consumption optimization comes from the fact of well-balanced propagation delay. This feature is advantageous for applications in which the skew between arriving signals is critical for proper operation, and for cascaded applications to reduce the chance of making glitches [2].

4) Power-ground-free main structure leads to power reduction.

5) Symmetrical structure, high modularity, and regular arrangement of designs give rise to sharing more wells of connected transistors and in turn reducing the occupied area about 26%–32%.

6) The degradation in all output voltage swing can thus be completely removed, which makes the design sustainable in low \( V_{DD} \) operations and low static power dissipation.

7) Internal logic structure of designs has the potential to be energy-efficient about 17%–53% due to the combined reduction of power consumption and propagation delay.

8) SCDM utilizes the benefits of different logic styles as the hybrid style [2].

9) The methodology has high flexibility in target and systematically consider it in the three design steps. This can lead to
efficient circuits in terms of performance, power, PDP, EDP, area, or a combination of them.

10) The fast evolution of microelectronics fabrication processes demands a new cell library generation or a library technology migration. The well-organized systematic methodology leads to automated flows, which can reduce design time and costs, provide consistency in the cell library generation process, increase the range of simulation capabilities at the characteristics step, as well as minimize the risk of errors [11], [12].

The rest of this brief is organized as follows. Previous work is reviewed in Section II. The details of SCDM and the three-input XOR/XNORs as the outcome of findings are discussed in Section III. Simulation results are analyzed in Section IV. Finally, the conclusions are drawn in Section V.

II. PREVIOUS WORK

The state-of-the-art issues in this brief can be divided into two categories as they are extracted from the topic: 1) conventional three-input XOR and 2) methodologies. Most of the designed SUMs have been produced jointly or by cascading some modules. The cascaded modules derived from reformulations of the Boolean function, such as

$$\text{SUM} = C_{\text{in}} \oplus H$$

(1)

$$\text{SUM} = C_{\text{in}} : H' + C_{\text{in}} \cdot H$$

(2)

$$\text{SUM} = C_{\text{in}} : H' + C_{\text{out}} \cdot H, \quad C_{\text{out}} = C_{\text{in}} \cdot H + A \cdot H'$$

(3)

where H and H' are A \oplus B and the complement of H, respectively. In (1), the H output is XORed with carry of the previous stage (C_in). The SUM modules belonging to this category have been utilized in many adders, such as SRF, XOR-FA, 9A, and 9B as SUM module [13], [14]. Expression (2) can be realized with a two-to-one multiplexer with H and H' as the select lines, which is widely used in adder implementation, such as Hernandez1, Hernandez2 [2], 10TFA, TFA, 14T, 16T [13], NEW14T [15], HPSC, NEWHPSC [6], and New-Hybrid [5]. In (3), carry from the previous and this stage, C_in and C_out besides H and H' are employed to generate SUM output. LPFS-FA [1] is made up of the expression as a SUM module. Finally, as mentioned before, some circuits jointly produced the module from which we can point to three-XOR, new-three-XOR [16], SUM-bridge, SUM-PTL, 10T_new, 12T_new, and 18T_new_FS [3]. Among all of the mentioned circuits, we consider the SUM modules of Hernandez1, Hernandez2, TFA, Hybrid, NEWHPSC, LPFS-FA, and 18T_NEW_FS, whose excellent performance are confirmed in [1], [2], and [4]–[6]. As a result, the complete comparison will occur by selecting them for reference. As can be observed from the conventional circuits, all the published efficient designs rely on creative ideas of designers. They do not follow a systematic approach, whereas new solutions often have improved few characteristics, and so there is a free space for the systematic design methodology. CDM has been utilized to design some limited functions [7]–[9]. In this brief, CDM is matured for the systematic design methodology. CDM has been utilized to often have improved few characteristics, and so there is a free space in terms of PDP is presented in Section III-B. In the last step, in order to put the resultant circuits in proper state, a sizing algorithm consistent with the methodology is indispensable. In this line, SEA algorithm that is simple exact algorithm with the capability of determining goal is picked [17].

A. Elementary Basic Cell Systematic Generation

In order to generate the EBC of three-input XOR/XNOR circuits, four steps are taken. The process has been shown in Fig. 1(b)–(e). Initially, three-input XOR and its complement is represented by one binary decision tree (BDT) [18] in order to share common subcircuits. The BDT is achieved by some cascaded 2 \times 1 MUX blocks, which are denoted by simplified symbol controlled with input variables at each correspondent level. This construction simply implements the minterms of the three-input XOR/XNOR function, as shown in Fig. 1(b). The step is followed by applying reduction rules to simplify the BDT representation. These include elimination, merging, and coupling rules. The major task of the coupling rule, in simple terms, is to obtain all the possible equivalent trees by interchanging the order of the controls. The trees are acquired by impacting the state matrix on the corresponding control matrix where the multiply and add operators operate as follows [19]:

$$0^t \chi_1 = \chi$$

$$1^t \chi_1 = \chi$$

$$\chi_1 \chi_2 \cdots \chi_m = \chi_1 \chi_2 \cdots \chi_m = 11 \cdots 1 = I_{2^m - 1}.$$

The result of applying the reduction rules to the tree is shown in Fig. 1(c). Afterward, as the inputs into the first level are 0’s and 1’s of the function’s truth table, the 0 and 1 can be replaced by the Y and Y', respectively. Finally, the simplified symbol can be divided into two distinct symbols: 1) the plus sign with the x input control and 2) the minus sign with the x' input control. The result of applying steps 3 and 4 is shown in Fig. 1(d). The EBC, which is extracted from the above procedure, has been presented in Fig. 1(e). This cell has eight elements, deciding two outputs. We refer to the pins of the central section (IN1–IN4 and G1–G4) as A or C, or their complements. We also assume that pins of the external section G5–G8 can also be B or its complement.

B. Wisely Selection of Mechanisms and Cells Based on Design Target

By replacing the elements with pass transistors or transmission gates and the control inputs with input signals in combination with optimization and correction mechanisms, a huge circuit library is achieved as each circuit can be appropriate for specific applications. The selection is mediated to determine dominant mechanisms and cells, in terms of PDP, power, and delay when the optimization goal is PDP. The results are used to produce
circuits for high-performance portable electronic applications. Mechanisms include optimization mechanisms to resolve nonfull swing [inverter (I) and feedback (F)], correction mechanisms to resolve high impedance [pull up-down network (P) and feedback (F)], or the combinations of them [bootstrap-pull (BP) up-down, feedback-pull (FP) up-down, bootstrap-feedback (BF), inverter-feedback (IF), and inverter-pull (IP) up-down]. The cells are divided into three categories: 1) cells with both nMOS and pMOS in EBC structure (C1); 2) only nMOS (C2); and 3) only pMOS (C3).

To reduce complexity, we have also considered the central part of EBC and to achieve real results, the circuits have been simulated in the chain test bench [7]. The circuits have been named with the abbreviation of the mechanism (or cell) being utilized, while the other circumstances, cells, or mechanisms are assumed to be fixed.

Using transmission gates in EBC, which is called TG, the complete circuit is achieved as there is no need for any other mechanisms. Therefore, TG is compared separately with others. Fig. 2(a) shows the order of mechanisms in terms of average power and PDP in voltage range from 0.6 to 2 V. If the concentration is on delay consumption, the right chart can be useful [Fig. 2(b)]. Fig. 2(c) also shows the PDP details for different mechanisms.

The first experiment that studies the performance of the inverter mechanism shows I suffers from more power and PDP in comparison with other mechanisms. The PDP details of I in Fig. 2(c) also demonstrate that there is an inconsistency with the voltage reduction in the mechanism as I has the minimum supply voltage of 0.8 V. The P mechanism is combined with the B or I to resolve high impedance. As can be observed from Fig. 2, IP consumes 1.33 ×, 1.11 ×, and 1.61 × more average power, delay, and PDP than BP, respectively. The increase in the static power consumption and switching delay of I are due to nonfull swing drive of the inverter. However, BP brings advantages in power reduction using blocking voltage in intermediate nodes to shift the gate voltage. The combined mechanisms, IP and BP, result in 26%–44%, 14%–23%, and 19%–44% improvement in power, delay, and PDP, respectively, compared with I. The next experiment extends to investigate transistors’ area of the mechanisms rather than the basic cells when the difference in circuits is their utilized mechanisms. We roughly estimated the transistors’ area by adding the area (W × L) of all the transistors that is \( \sum W_i L_i \). Fig. 3(a) shows the transistors’ area of basic cell (BCTA), bootstrap (BTA), feedback (FTA), pull up-down (PTA), and inverter (ITA). Although the number of mechanism transistors in some cases is more than the basic cell transistors, BCTA occupies the most area in the majority of circuits. This is because the mechanism transistors are responsible for gate driving, such as in B, or resolving high impedance of only some states, such as in F and P, which are weaker responsibilities compared with that of the cell transistors for output generation. Therefore, the sizing algorithm also tends to choose the mechanism transistors’ area to be smaller than BCTA.

In the next experiment, we address feedback mechanism. The F network, when the cell is meditating to change the outputs, tries to keep the previous state, which gives rise to a struggle. This initial struggle causes the voltage step, as well as delay and power to increase. Therefore, the sizing algorithm chooses small sizes for F transistors not to be dominated. This choice leads to the scenario that F outperforms I by consuming 25%, 45%, and 48% less in power, delay, and PDP, respectively (Fig. 2). The struggle will be more critical when the F transistors are driven by the nonfull swing outputs or they should resolve solely the high impedance problem, because they should be strong enough to do the duty. The stronger the F transistors, the more the struggle and their consequences are more likely to happen. As a result, in these cases, it is better that high impedance duty is solved by B. As we can observe from Fig. 2, the mechanisms IP, BP, and FP use P for high impedance and exhibit a power saving of 2%–34% and a PDP improvement of 5%–57% rather than both IF and BF. The last experiment investigates the basic cells to characterize the cell, which outperforms in all mechanisms. Fig. 3(b) shows the average PDP of the mentioned three groups of cells against the combinational mechanisms. According to the figure, C2 with the most numbers of nMOS transistors in its structure enjoys better results. The worst one is C3 with the largest number of pMOSs.

Taken all the above points together, under the assumptions about the technology and the domain of circuits, the individual mechanism, I, does not present proper performance in terms of power and delay. This is while I was introduced as the only solution for nonfull swing outputs in many papers. Due to the high power consumption, I in combinational mechanism, such as IF and IP, operate worse than both BF and BP. The high impedance problem is also better resolved by P as we can observe IP to IF and BP to BF perform superior. Next, using transmission gate in EBC and TG enjoys the least power, delay, and PDP as a complete part that does not need any mechanisms. In the end, the individual mechanism, F, with suitable transistor sizing is capable of playing a key role besides the dominant combinational mechanisms, BP and FP, for the wisely design when PDP is target. Based on the findings, circuits with names XO1 through XO10 are presented, whose the building structure details with the average PDP are tabulated in Table I.
TABLE I
INTRODUCTION OF THE STRUCTURE OF THREE-INPUT XOR/XNOR CIRCUITS WITH THE AVERAGE PDP IN FEMTOJOULE

<table>
<thead>
<tr>
<th>Circuits</th>
<th>MECHANISMS</th>
<th>F</th>
<th>B</th>
<th>P</th>
<th>MECHANISMS</th>
<th>F</th>
<th>B</th>
<th>P</th>
<th>AVG PDP</th>
</tr>
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<tbody>
<tr>
<td>XO1</td>
<td>TG</td>
<td>C1</td>
<td>PNP</td>
<td>-</td>
<td>-</td>
<td>1.27</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>XO2</td>
<td>C2</td>
<td>FNP</td>
<td>1</td>
<td>-</td>
<td>-</td>
<td>0.70</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>XO3</td>
<td>TG</td>
<td>C2</td>
<td>PNP</td>
<td>-</td>
<td>-</td>
<td>0.62</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>XO4</td>
<td>TG</td>
<td>C1</td>
<td>PNP</td>
<td>-</td>
<td>-</td>
<td>0.42</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>XO5</td>
<td>TG</td>
<td>C1</td>
<td>PNP</td>
<td>-</td>
<td>-</td>
<td>0.71</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>XO6</td>
<td>C2</td>
<td>FNP</td>
<td>1</td>
<td>-</td>
<td>-</td>
<td>0.57</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>XO7</td>
<td>TG</td>
<td>C1</td>
<td>PNP</td>
<td>-</td>
<td>-</td>
<td>0.47</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>XO8</td>
<td>TG</td>
<td>C1</td>
<td>PNP</td>
<td>-</td>
<td>-</td>
<td>0.86</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>XO9</td>
<td>C2</td>
<td>FNP</td>
<td>1</td>
<td>-</td>
<td>-</td>
<td>0.65</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>XO10</td>
<td>TG</td>
<td>C2</td>
<td>-</td>
<td>n</td>
<td>-</td>
<td>0.50</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Fig. 4 shows XO4, XO7, and XO10 of the proposed circuits.

TABLE II
SIMULATION RESULTS (POWER IN MICROWATT, DELAY IN NANOSECOND, PD IN FEMTOJOULE, AND STATIC AND PARITY CHECKER IN 1.2 V)

<table>
<thead>
<tr>
<th>Circuits</th>
<th>avg PDP</th>
<th>avg pwr</th>
<th>avg dy</th>
<th>avg ED</th>
<th>static PDP</th>
<th>static dy</th>
<th>Parity Checker</th>
</tr>
</thead>
<tbody>
<tr>
<td>XO4</td>
<td>0.42</td>
<td>2.99</td>
<td>0.19</td>
<td>0.08</td>
<td>0.0025</td>
<td>2.00</td>
<td>0.33</td>
</tr>
<tr>
<td>XO7</td>
<td>0.47</td>
<td>3.17</td>
<td>0.19</td>
<td>0.09</td>
<td>0.0030</td>
<td>2.04</td>
<td>0.32</td>
</tr>
<tr>
<td>XO10</td>
<td>0.50</td>
<td>3.07</td>
<td>0.22</td>
<td>0.11</td>
<td>0.0024</td>
<td>2.03</td>
<td>0.30</td>
</tr>
<tr>
<td>Hernandez1</td>
<td>0.51</td>
<td>3.08</td>
<td>0.21</td>
<td>0.11</td>
<td>0.0022</td>
<td>2.08</td>
<td>0.40</td>
</tr>
<tr>
<td>TF</td>
<td>0.52</td>
<td>2.79</td>
<td>0.23</td>
<td>0.12</td>
<td>0.0017</td>
<td>2.40</td>
<td>0.35</td>
</tr>
<tr>
<td>18T_new_FS</td>
<td>0.52</td>
<td>2.75</td>
<td>0.24</td>
<td>0.12</td>
<td>0.0022</td>
<td>2.66</td>
<td>0.38</td>
</tr>
<tr>
<td>Hernandez2</td>
<td>0.62</td>
<td>3.11</td>
<td>0.25</td>
<td>0.16</td>
<td>0.0022</td>
<td>2.93</td>
<td>0.43</td>
</tr>
<tr>
<td>HYBRID</td>
<td>0.63</td>
<td>2.61</td>
<td>0.29</td>
<td>0.18</td>
<td>0.0011</td>
<td>2.72</td>
<td>0.46</td>
</tr>
<tr>
<td>LBPHS-FA</td>
<td>0.76</td>
<td>2.56</td>
<td>0.38</td>
<td>0.09</td>
<td>0.0010</td>
<td>2.78</td>
<td>0.48</td>
</tr>
<tr>
<td>LPHS-FA</td>
<td>0.91</td>
<td>3.41</td>
<td>0.38</td>
<td>0.35</td>
<td>0.0012</td>
<td>2.84</td>
<td>0.40</td>
</tr>
</tbody>
</table>

Fig. 4 shows XO4, XO7, and XO10 of the proposed circuits.

IV. SIMULATION RESULTS
To investigate and compare the performance of the proposed circuits, seven SUM modules with complementary outputs of full adders (FAs), TFA, Hernandez1, Hernandez2, NEWHPSC, Hybrid, 18T_new_FS, and LPHS-FA have been chosen, whose excellence have been confirmed in [1], [2], and [4]–[6]. Therefore, an approximately fair comparison will take place by selecting them. In general, the simulation setup and testbench suggested in [2] are utilized. All the circuits are simulated using the BSIM3v3 model (level 49) in HSPICE based on the TSMC 0.13-m CMOS technology and to a fair evaluation sized using SEA [17] for PDP in 0.8–1.6 V. DD. To measure the sensitivity to circuit noise, the noise immunity curves (NICs) are used, which is the locus of points (T noise and V noise), where T noise and V noise correspond to the noise pulsewidth and amplitude, respectively. All the points below the NIC fall in a safe zone. For quantitative evaluation, a metric derived from the NIC is given by $ANTE = E(V_{noise}^2)$. Hence, the higher the NIC of a gate and ANTE value, the less susceptible is the gate to noise [4], [20].

To control the volume of this brief, only the simulation results of the conventional and three of the best proposed circuits in terms of average PDP according to Table I, XO4, XO7, and XO10, are tabulated in Table II. The ascending order of delay, which is the maximum delay between all the possible transitions, as well as PDP are also shown in Fig. 5(a). It is apparent that among the circuits, XO4 and XO7 have the smallest delays. XO7 has slightly less delay than the XO4 at lower supply voltages. However, the trend will reverse at higher supply voltages. Hernandez1 has the second position. The circuits XO10, TF, and 18T_new_FS follow the Hernandez1. In the common circumstances, the circuits utilizing FP, such as XO7 is superior to the circuits utilizing BP like XO10, which is compatible with the delay trend of mechanisms in Fig. 2. The circuits with C2 like XO10 and XO7 also perform better than the circuits with C1. Since bootstrap technique saves the internal node voltages, the average power dissipation under different supply voltages shows that PB has less power dissipation in common situation. XO10 employing BP outperforms XO7 employing FP with regard to average power. According to the PDP trend in Fig. 2, the ability of TG to provide full-swing leads to the best circuit with optimum performance and drivability as among the circuits, XO4 has the lowest PDP. After that, circuits XO7 and XO10 have the second and third position, respectively. PDP of XO7 is less than that of XO10 for lower voltages but the trend reverses for higher voltages. Hence, from energy point of view, XO7 is a better choice. The circuits, such as XO7 using FP outperform the circuits using F. The circuits with C2 like XO7 and XO10 offer less PDP than the circuits with C1. The similar PDP trend can be observed in parity checker test bench. Taken all the above points together, the results of Hernandez1 and TF approach to that of XO4 because of some similarity in their structures. This similarity can be also observed in Hernandez2 with XO3 and HYBRID structures, NEWHPSC with XO5. Finally, since LPHS-FA uses carry module to generate SUM in the three-input XOR, it is not in a good position in terms of PDP except in a FA structure. In the optimum state from transistor sizing point of view, six dominant circuits are XO4, XO7, XO10, Hernandez1, TF, and 18T_new_FS for which some extra investigation are performed. The evaluation results are summarized in Table III. In Fig. 5(b), power-delay curve
for the six top circuits for different voltages. The points on the bottom leftmost corner of the graph indicate good PDP zones. As we can observe, all the points of XO4, XO7, and XO10 are around the bottom leftmost corner to achieve the minimum PDP in each voltage.

Unbalanced outputs lead to more spurious transitions to the cascaded stage. Then, for quantitative evaluation of the delay difference between two outputs and determining amount of the simultaneous generation, a metric called normalized delay difference (δ) was defined

\[
\delta = \frac{\text{Max}(t_{\text{XOR}}_3, t_{\text{XNOR}}_3) - \text{Min}(t_{\text{XOR}}_3, t_{\text{XNOR}}_3)}{\text{Max}(t_{\text{XOR}}_3, t_{\text{XNOR}}_3)}
\]

(4)

where the \(t_{\text{XOR}}_3\) and \(t_{\text{XNOR}}_3\) values are larger and smaller delay between \(t_{\text{XOR}}_3\) and \(t_{\text{XNOR}}_3\) outputs, respective[6]. The smaller δ, the less glitch with less amplitude and less width probably is in outputs. In Fig. 5(c), the δ values show that the outputs of the proposed circuits are more balanced especially at low voltages. Fig. 5(d) shows the NIC of six of the best and the previous ones. The curves and ANTE in Table III indicate the proposed circuits enjoy more noise immunity as compared with the others. Driving capability of the circuits in different fan-outs are shown in the table realizing the overall delay of XO10, XO4, TF, and XO7 are much lower, while 18T_new_FS and Hernandez1 do not operate in the higher fan-outs. The new designs also work at higher frequencies. Fig. 6 shows the layout occupied by each three-input XOR/XNOR considered at 1.2 V. Among the circuits, the XO4 has the lowest area and enjoys 26%–32% improvement (Table III). The density determines the number of transistors in an area unit, which is more in new designs. This is attributed to the high modularity and complete symmetric and regular arrangement of transistors. These enable more sharing of the connected transistor wells and, therefore, occupy less area. The area can also be considered as one of the factors for presenting lower delay and power consumption, as it implies smaller parasitic capacitances being driven inside the FA.

V. CONCLUSION

SCDM serves as a design methodology for three-input XOR/XNOR, which is one of the most complex and competitive as well as all-purpose three-input basic gates in arithmetic circuits. The methodology puts emphasis on doing all the steps in a completely systematic way. It also enjoys high flexibility in design target, while it follows the same procedure to obtain the state-of-the-art designs. This brief has favored SCDM with the wise selection of the circuit components for the PDP target. In the end, three new high performance three-input XOR/XNOR circuits with less PDP and occupied area are conceived using SCDM. The new circuits enjoy higher driving capability, transistor density, noise immunity with low-voltage operation, and the least probability to produce glitches. As a unique feature, the critical path of the presented designs consists of only two transistors, which causes low propagation delay. On average, these circuits outperform their counterparts with 17%–53% and 27%–77% improvement in PDP and EDK, respectively, in HSPICE simulation based on the TSMC 0.13-μm technology. The area utilization for the proposed circuits enjoys 26%–32% improvement with the advantages of regularity and symmetry in layout.

REFERENCES


