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Using Boolean Tests to Improve Detection of Transistor Stuck-open Faults in CMOS Digital Logic Circuits

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Abstract – Currently transistor stuck-open (TSOP) faults in CMOS digital logic circuits are detected by two pattern tests consisting of an initialization pattern to set the output of a faulty gate followed by a pattern that detects a stuck-at fault. Some TSOP faults may not be detected by such two-pattern tests. One reason for this is that appropriate initialization patterns cannot be obtained using Boolean (steady state) analysis of the circuit. For some of these faults, required initialization may be possible using hazards (glitches) [10][13]. However, insuring that a test using hazard-based initialization actually detects the target fault requires accurate transient analysis of the circuit under test such as by SPICE.

In this work we propose methods to augment test generation procedures to detect TSOP faults using traditional steady state Boolean analysis (called *Boolean tests* in this work). We also investigate the cause for the non-existence of tests for the faults not detected in benchmark circuits. In many such cases we found that the non-existence of test patterns is due to redundant gates that can be replaced by a constant 1 or 0. We present results on larger ISCAS-89 benchmark circuits to illustrate the effectiveness of the proposed methods to generate tests to detect TSOP faults and the results of analysis for the non-existence of tests for the remaining faults undetected by Boolean tests.

Key words: Transistor stuck open faults, fault detection tests, multi-cycle tests.

1. Introduction

A type of fault in CMOS digital logic circuits, called *transistor stuck-open* (*TSOP*) fault, has been extensively studied [1]-[3] since its introduction by Wadsack in 1978 [1]. By a TSOP fault we mean a transistor, an NFET or PFET, is permanently off and cannot be turned on by applying appropriate logic value to the gate terminal of the transistor. Studies of methods to generate tests to detect transistor stuck-open faults were motivated by results on test of manufactured digital CMOS VLSI circuits [4][5]. These results on defects in real silicon showed the existence of defects that were detected by two-pattern tests using low frequency capture cycles and were called sequence dependent and timing independent (SDTI) faults [4][5]. Diagnosis of the failing chips in the Murphy chip test experiment [4] revealed that the defects in several chips were TSOP faults. A recent study showed that use of what are called cell aware tests detected several defects not detected by stuck-at and transition delay faults [6][7]. In this study, analysis of the coverage of defects internal to the cells of an automobile electronic chip showed that the test sets based on the classical line stuck-at and gate delay faults missed cell internal faults such as TSOP faults and interconnect opens which were detected by the cell aware tests [7]. Based on these silicon experiment results, methods to generate tests to detect TSOP faults were revisited in [8]-[11].

Methods to generate tests for TSOP faults using ATPGs for transition delay faults were investigated in [8][9]. In [10][11] tests to detect TSOP faults using hazards (glitches) to initialize the output of the gate containing the faults were investigated. Such tests are meant to supplement the two-pattern tests based on steady state values to detect additional TSOP faults. Tests that are based on hazards may require validation using accurate timing waveform yielding simulators such as SPICE and hence may be difficult to derive for large circuits. Furthermore process variations may effect accuracy of hazard calculations.

Motivated by the potential difficulty in ascertaining detection by hazard based tests, in this paper we consider generation of tests that achieve high coverage of TSOP faults based on steady state logic values as is typical of currently used ATPGs for line stuck-at and delay faults. We call such tests *Boolean tests* and the results presented in this paper for larger ISCAS-89 benchmark circuits demonstrate that Boolean tests may achieve very high coverage of TSOP faults.

The remainder of this paper is organized as follows. In Section 2 we discuss currently used tests for TSOP faults together with a brief review of related work. In Section 3 we describe the Boolean tests we propose to achieve high coverage of TSOP faults. Section 4 presents experimental results on coverage of TSOP faults by the proposed tests for larger ISCAS-89 benchmark circuits. We also present results of our study of the causes for non-existence of Boolean tests for some TSOP faults. Section 5 concludes the paper.

2. Preliminaries

For the sake of simplicity, in this paper, we assume that the circuit for which tests are generated is a scan design composed of primitive gates NOT, NAND, and NOR.

Consider the NAND gate shown in Fig. 1 and a two-pattern test for it shown in Fig. 2(a). Let the PFET connected

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to input *A* be stuck-open. If *A*=0 and *B*=1 is applied to the NAND gate, the output *Z* will be in high impedance or floating state instead of being 1 as no conducting path to VDD or ground will exist. The logic state of Z will thus be unknown. For this reason one has to initialize the gate output *Z* to a known value. For the stuck-open fault under consideration, *Z* has to be initialized to 0 by applying input *A*=1 and *B*=1. Next, if the input *A*=0 and *B*=1 is applied, output *Z* will be 0 instead of the fault-free value 1 since the floating output node retains its previous value. When the gate is part of a larger circuit the faulty value 0 instead of fault-free value 1 must be propagated to an observed output and this will require input *A* stuck-at-1 test which is also the output stuck-at-0 test. Thus, detecting TSOP faults requires test patterns that initialize the gate output to a known value followed by inputs that will set the gate output to high impedance or floating state and propagate the fault effect using an appropriate line stuck-at test.

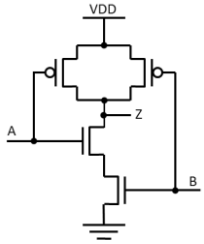

Fig. 1: A two input NAND gate

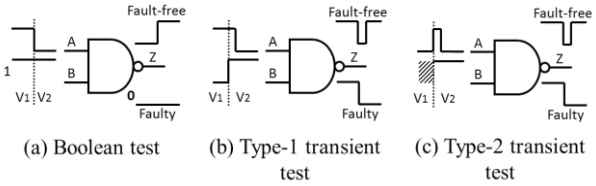

Fig. 2: Boolean and transient tests

Consider the same PFET TSOP fault as above and the inputs shown in Fig. 2(b). The input *A* is initially at 1 and changes to 0 and input *B* is initially 0 and changes to 1. If *B* changes before *A* both inputs to the NAND gate will be 1 for a time causing the output *Z* to become 0 and when *A* changes to 0 the output will be in high impedance state and remains at 0, the value it was at immediately preceding *A* changing to 0. As can be seen in the fault-free circuit the output *Z* has a 1-hazard that causes the output to be 0 for a time. Of course the occurrence of this hazard and its length that initializes the output to 0 depends on the relative times at which *A* and *B* change and the inertial delay of the NAND gate. For testing for the TSOP fault when no test as illustrated in Fig. 2(a) exists the type of test illustrated in Fig. 2(b) may exist and should be used to achieve higher coverage of TSOP faults. A test which initializes the output of the NAND gate to zero followed by driving the output to high impedance state by a hazard on input *A* is illustrated in Fig. 2(c). In this work we call the tests that are based on steady state values *Boolean tests*. The test shown in Fig. 2(a) is an example of a Boolean test. We refer to the tests that use hazards to initialize the gate outputs to known value as *Transient tests.* The two types of transient tests illustrated in Figures 2(b) and 2(c) are called Type-1 and Type-2 transient tests, respectively.

Type-1 tests create hazard in the gate with the TSOP fault and Type-2 tests create hazards prior to the gate with the TSOP fault. In [10][11] the transient tests were considered for TSOP faults that could not be detected using Boolean tests illustrated in Fig. 2(a). The Boolean and transient tests illustrated in Fig. 2 are two-pattern tests and are closely related to tests for transition delay faults (TDFs). Hazard based tests for delay faults were considered in [12][13] . For example all three tests of Fig. 2 are tests for slow-to-fall fault on input *A*. In practice, the ATPGs for TDFs generate the Boolean tests or Type-1 transient tests for TDFs. This correspondence between tests for TDFs and TSOP faults has been used to generate Boolean tests to detect TSOP faults in [8][9], where circuits were modified at the faulty gate to derive tests for TSOP faults using ATPGs for TDF faults. The circuit modifications insure that the output of the fault-free gate makes a state transition as in Fig. 2(a) to obtain Boolean tests for TSOP faults that are also TDF tests. Since modifying circuits for each targeted fault is typically expensive in compute time we propose adding extra conditions on the inputs to faulty gates to derive tests to detect TSOP faults using ATPGs for TDFs. This is discussed in the next section.

Next we discuss reasons for the non-existence of Boolean tests while Type-1 and/or Type-2 transient tests may exist to detect TSOP faults. First, note that the tests to detect TSOP faults must be at least two-pattern tests, to initialize the output of the faulty gate followed by a test for a stuck-at fault. Both for Boolean and transient tests, the pattern that detects the TSOP fault must detect a stuck-at-1 (stuck-at-0) fault at the input of the faulty gate in order to detect a PFET (NFET) stuck-open fault. Thus the first difference between the Boolean and transient tests is that Boolean tests need an initializing steady state input to the faulty gate whereas the transient tests initialize the gate output using hazards. Next, we observe that for standard scan designs two-pattern tests use launch-off-capture (LOC) [14] and/or launch-off-shift (LOS) tests [15]. In both LOC and LOS tests, the second pattern is a function of the first pattern. This may preclude application of a required stuck-at test pattern, to detect a TSOP fault, immediately following the initializing input. In the first case where a steady state initializing input does not exist it implies that the gate output is a constant for all inputs or the gate is a redundant gate. For example if the output of a NAND gate cannot be initialized to zero it implies that the gate output remains at one for all inputs. In other words non-existence of Boolean tests for TSOP faults in these cases is due to redundant logic. For the second case where two pattern tests to detect TSOP faults do not exist because the required stuck-at test cannot be obtained immediately following the initializing input, it may be possible to obtain tests with three or more patterns. We demonstrate this in the next section together with conditions that need to be satisfied by such tests for scan designs.

Another typical restriction imposed on multi-pattern tests for standard scan designs is that the primary inputs (PIs) of the circuit are held constant during the application of

functional clock cycles after the initial state is scanned in. This restriction is enforced for at-speed test for delay faults. However, it is not required for the detection of TSOP faults. Experimental results we present in Section 4 show that relaxing the requirement to hold PIs constant after scanning in the first pattern of a multi-pattern test increases TSOP fault coverage considerably.

One point that is important to make regarding tests for TSOP faults is the following. All the tests shown in Fig. 2 and also those considered later may be invalidated by hazards if they discharge (charge) the output of the gate with the TSOP fault initialized to 1 (0) [16]. For example in Fig. 2(b) if there is a 1-hazard on B causing B to have a glitch of 0 after A goes to zero it can charge the NAND gate output to 1 which is the fault-free value and hence the targeted TSOP fault is not detected. However such test invalidation can be avoided by insuring robust initialization of the gate with the fault [16]. We do not consider this issue further in this work.

3. Proposed Test Generation Methods for TSOP Faults

In this section we discuss the Boolean tests we propose for enhancing TSOP fault coverage. In Section 3.1 we discuss launch-off-capture (LOC) and launch-off-shift (LOS) tests. In Section 3.2 we discuss multi-cycle tests we propose. In Section 3.3 we discuss changing primary inputs of the circuit during LOC and LOS tests. In Section 3.4 we discuss how we determine the TSOP faults to be targeted by the proposed test generation methods.

3.1. LOC and LOS tests to Detect TSOP Faults

For standard scan designs two-pattern tests are applied using LOC [14] or LOS [15] test application methods. Traditionally, these tests are used to detect delay faults such as TDFs, small delay defects and path delay faults.

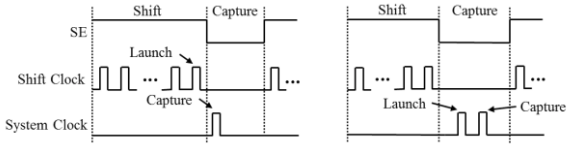

Fig 3: Timing diagrams of LOS and LOC

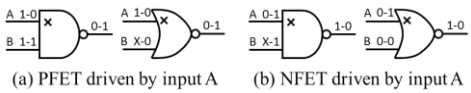

Fig. 4: Two-cycle Boolean tests for TSOP faults

For the sake of completeness, next we briefly discuss LOC and LOS tests. The timing diagrams for the applications of these tests are shown in Fig. 3. Both types of tests are applied by scanning in, with the scan enable signal asserted (high), the sequential state part of the test inputs to the combinational circuit of the scan design. This input initializes the fault site. In LOS tests, typically, the last scan shift cycle is used to apply the first pattern of the two-pattern test with scan enable asserted. This cycle is referred to as the launch cycle. Then the scan enable is de-asserted (made low) and a system clock cycle is applied to capture the response of the circuit. In LOC tests after the first pattern is scanned in, two system clock cycles are applied with scan enable de-asserted (cf. Figure 3(b)) to launch the second pattern and capture the test response. In order to facilitate at-speed test in LOS the scan enable signal has to be fast and typically requires additional design effort and/or DFT [17]. Also to facilitate use of low cost testers for at-speed test the launch and/or capture clock cycles are typically generated using on-chip PLLs. For this reason the primary inputs of the circuit under test cannot be changed from the external ATE after initializing the circuit. However for TSOP faults, at-speed test is not needed since the output of the gate with a TSOP fault can be expected to retain the initialized value for several cycles of a slow clock applied from the ATE and used for launch and capture. This also allows changing the primary inputs during launch and capture cycles. Experimental results presented in the next section show that allowing primary inputs to change as discussed above facilitates achieving much higher TSOP fault coverage.

In Fig. 4 we give the inputs to NAND and NOR gates for the two-pattern Boolean tests to detect PFET and NFET TSOP faults connected to input *A*, where X implies that the Boolean value can be 0 or 1. We enhanced a commercial ATPG for TDF tests to derive TSOP tests by requiring it to generate tests that satisfy the conditions shown in Fig. 4.

3.2. Multi-Cycle Tests

As discussed earlier traditional TSOP test generation uses two-cycle tests. In Fig. 5, the PFET SOP fault inside the NAND gate can only be detected by the LOS two-cycle Type-1 transient test. However, the extra buffer between DFF_2 and *g* causes the rising transition arrive later than the falling transition originated from DFF_1, which makes the Type-1 transient test become invalid. When we apply the LOC test shown in Fig. 5, it can be easily verified that the SOP fault is detected. This LOC test is a three-cycle Boolean test.

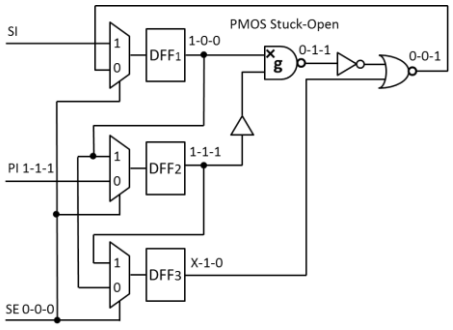

Fig. 5: Two-cycle test for PFET SOP fault

The example shown in Fig. 5 implies that the state dependency between two adjacent cycles prevents from generating two-cycle Boolean test. However, inserting one or more additional cycle(s) between the launch cycle and the capture cycle relaxes the state dependency that makes the TSOP fault to be detected by the Boolean test.

In Fig. 6, we show the N-cycle Boolean tests for NAND and NOR gates for FETs driven by input *A*, where the value in square brackets is repeated N-2 cycle(s).

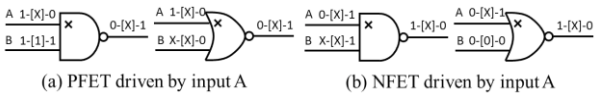

Fig. 6: N-cycle Boolean tests for TSOP

3.3. N-Cycle Tests without Holding PIs

Test generation with holding PIs during launch and capture cycles renders some testable TSOP faults become untestable. In Fig. 7, the PFET SOP fault inside NAND gate driven by the input *A* is untestable if PI_2 holds its value during capture. Allowing PI_2 to change from 1 to 0, the LOC Boolean test shown in Fig. 7 detects this fault. Similarly, both the PFET and NFET TSOP faults inside NOR gate driven by the primary input PI_2 are untestable when holding PI_2. Allowing it to change value makes both TSOP faults testable. Since the TSOP fault is a clock frequency independent fault model, the stuck-at test configuration of the external ATE can be used to generate tests for the TSOP faults, where holding PI is not enforced during test generation and application.

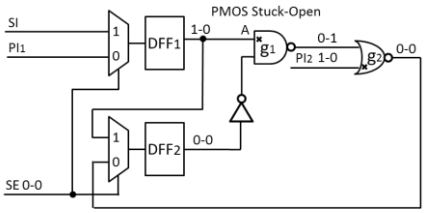

Fig. 7: Testable TSOP faults without holding PIs

In our experiments on generating N-cycle Boolean tests without holding PIs, we start N from 2. If current N-cycle Boolean test does not exist for the target fault, N is increased by 1 till the fault is detected or a predefined limit is reached.

It should be pointed out that in an earlier preliminary work we considered multi-cycle tests to detect TSOP faults [18]. However, the work in [18] used circuit modifications to derive the tests and also used stronger necessary conditions for the detection of TSOP faults as well as permitting circuit primary input changes during launch and capture cycles was not considered.

3.4. Upper Bound on Two-Cycle Detectable TSOP Faults

In the next section we give experimental results for TSOP fault coverage obtained by the tests described above. In order to assess the effectiveness of using the tests proposed in Sections 3.2 and 3.3 it will be useful to know the number of faults detectable by both the Boolean and transient two-pattern tests. Tools to generate two-pattern transient tests are not available to us and hence we use upper bounds on the number of TSOP faults that can be detected by two-cycle tests including transient tests. We determined an upper bound on the TSOP faults that can be detected by two-cycle Boolean or transient tests in the NAND, NOR, and NOT gates of the circuit under test as follows.

The total number of TSOP faults in the circuit with NAND, NOR, and NOT gates is equal to twice the number of inputs to the gates. Let the list of the corresponding faults be *F*. Since a PFET (NFET) stuck-open fault requires that the stuck-at-1 (stuck-at-0) fault on the gate input driving the PFET (NFET) is detectable we remove the TSOP faults corresponding to the undetectable line stuck-at faults from *F* to get a reduced list of faults *F'*. The TSOP faults in *F' may* be detectable by two-cycle Boolean or transient tests. Next we determine an upper bound on the TSOP faults that may be detectable by Boolean and/or Type-1 transient two-cycle tests using the following observation.

As shown in Fig. 2, the PFET TSOP fault inside NAND gate may be detected by either a Boolean test or Type-1 transient test. Tests of both these types detect the slow-to-fall transition faults at the NAND gate input *A*. On the other hand, the test for NFET TSOP fault inside NAND gate driven by *A* is the same as the test to detect the slow-to-rise transition faults at *A*. Based on these detection conditions, the upper bound on TSOP faults detectable by Boolean and/or Type I transient two-cycle tests is equal to the number of detectable TDF faults at the inputs of these gates. Let the corresponding list of TSOP faults be *F"*. Note that the faults in *F"* can be obtained by determining the detectable TDF faults at the gate inputs. In *F"* we included the TSOP faults corresponding to the TDF faults detected by two-cycle LOC and LOS tests where we allowed primary inputs to change in launch and capture cycles as the number of these faults is higher than if we did not allow the primary inputs to change. The faults in (*F'-F"*) can only be detectable, if at all, by Type-2 two-cycle transient tests. Our goal is to detect all and if not a maximum a number of TSOP faults included in *F"* and (*F'-F"*) using the proposed Boolean tests.

It should be mentioned that a TSOP fault in (*F-F'*) is corresponding to a redundant stuck-at fault at the gate input. No Boolean test exists for it, but it can be detected by a Type-2 transient test only if a hazard occurs at the faulty input and the non-controlling value assigned at all the gate inputs except the faulty input allows create a sensitization path from the gate output to an observation point. Hence an upper bound on TSOP faults that may be detectable only by Type-2 two-cycle transient tests includes the number of faults in (*F'-F"*) plus some faults in (*F-F'*) that meets aforementioned conditions.

In the next section we give the results on TSOP faults detected by the proposed Boolean tests. We also investigated reasons for the failure of Boolean tests to detect TSOP faults among the faults in *F"* and (*F'-F"*).

4. Experimental Results

We enhanced a commercial ATPG for TDF faults to obtain the results reported in this section. In Table 1 we report the results on the number of TSOP faults detected by the proposed Boolean tests out of the set of faults in *F"* (as discussed in Section 3.4 these are the faults detectable by Boolean and/or Type-1 transient tests using two-cycle LOC

Table 1: Results on TSOP faults detected using Boolean tests

Circuit	# Gates	# Chains	# F	# F'	# F''	# Det. (Hold PIs)		# Det. (No Hold PIs)		Det. % w.r.t. F''	# Abort	# Undet. Faults
						2-Cycle LOC/LOS	3-Cycle LOC/LOS	2-Cycle LOC/LOS	3-Cycle LOC/LOS			
S5378	3259	13	4874	4815	4802	3969	3975	4787	4787	99.69	0	15
S9234	6163	14	8802	8287	8284	7220	7609	8275	8275	99.89	0	9
S13207	9624	25	11573	11379	11322	10715	10962	11222	11222	99.12	0	100
S15850	11270	23	14642	14076	14052	11594	11864	14027	14028	99.82	0	24
S35932	20671	41	48816	42416	42416	32973	33008	42416	42416	100	0	0
S38417	26045	40	37116	36943	36722	36053	36216	36508	36508	99.42	2	214
S38584	23077	37	49902	47830	47511	41387	41768	47131	47131	99.20	1	380
Total			175725	165746	165109	143911	145402	164366	164367	99.55	3	742

Table 2: Analysis of faults in (*F'-F''*)

Circuit	# Faults (*F'-F''*)		# Det. Faults						# Abort	Overall	
	# Pot. Det.	# Constrained	3-Cycle	4-Cycle	5-Cycle	6-Cycle	7-Cycle	Total		# Det. Faults	Det. % w.r.t *F'*
S5378	7	6	1	0	0	0	0	1	0	4788	99.44
S9234	3	0	1	0	0	0	0	1	0	8276	99.87
S13207	51	6	34	3	2	1	0	40	0	11262	98.97
S15850	9	15	6	0	0	0	0	6	0	14034	99.70
S35932	0	0	0	0	0	0	0	0	0	42416	100
S38417	211	10	28	15	12	7	10	72	19	36580	99.02
S38584	198	121	69	31	26	18	9	153	0	47284	98.86

Table 3: Analysis of faults in *F'* that are not detected by Boolean tests

Circuit	# Undet. TSOP Faults	# Gates Including Undet. TSOP Faults	# Redundant Gate Output Stuck-at Controlled Value		# TSOP Faults inside Gates with Redundant Output Stuck-at Controlled Value
			Unable to Activate	Unable to Propagate	
S5378	15	10	4	0	8
S9234	9	6	2	0	4
S13207	100	89	5	1	12
S15850	24	18	6	0	11
S35932	0	0	0	0	0
S38417	214	175	5	0	10
S38584	380	205	134	9	286

or LOS tests without holding the primary inputs constant during launch and capture cycles). In Table 1 after the circuit names we show the number of gates, the number of scan chains we used, followed by the total number of TSOP faults in the circuits (the faults in the set *F*). Next we give the number of TSOP faults in the set *F'* which are the faults that can be potentially detected by Boolean and/or transient tests. Next we give the number of TSOP faults in the set *F''*. We use an incremental ATPG that first generates Boolean LOC and LOS tests for which primary inputs are held constant during launch and capture cycles followed by Boolean tests where the primary inputs are allowed to change during launch and capture cycles. In the next four columns, the numbers of faults in *F''* that are detected by this incremental ATPG when LOC and LOS tests are generated, whilst allowing changing primary inputs, with two and three cycles are given. In the following column the percentage of faults in the set *F''* detected by the Boolean tests of up to 3 cycles, whilst allowing changing of primary inputs, is given followed by the number of aborted faults and the total number of faults in *F''* that are not detected (including the number of aborted faults). In the last row of Table 1 we show the sum of the number of faults in sets *F''* of all circuits and the sum of all detected faults among them as well as the percentage of faults among them.

From Table 1 one can note that, in the aggregate 99.55% of all TSOP faults that are detected by Boolean and/or transient tests are detected by Boolean tests by using LOC and LOS tests with up to three cycles. Also from columns 7 and 8 of Table 1 it can be noted that using tests with 3 cycles a total of 145,402 faults are detected while 143,911 faults are detected using 2-cycle tests, both with primary inputs held constant during launch and capture cycles. Similarly, from columns 9 and 10 of Table 1 it can be noted that by allowing primary inputs to change during launch and capture cycles the total number of faults detected increases from 145,402 to 164,367. We also attempt to generate LOC and LOS tests with that larger than three capture cycles whilst not allowing change in primary inputs. These tests failed to detect any faults beyond those reported in Column 8 of Table 1. Later in Table 3 we give results of an analysis of the undetected faults given in the last column of Table 1.

We next considered the faults in (*F'-F"*) which are the TSOP faults if detectable can only be detected by Type-2 transient 2-cycle LOC or LOS tests. Results for these faults are given in Table 2 in which after the circuit name we give the number of faults in (*F'-F"*) separated into two groups, followed by the number of faults detected by LOC and/or LOS Boolean tests with 3 and up to 7 cycles in which circuit primary inputs were allowed to change during capture cycle. The second group of faults whose number is given in column under # *Constrained* of Table 2 are inputs driving the faulty FET which remain constant for all inputs. That is, the gates driving these inputs can be replaced by constants. Such faults cannot be detected by Boolean tests. The faults whose number is given in column *under # Pot.* of Table 2 are potentially detectable by Boolean tests and the results on their detections are given in columns 4 through 10 of Table 2. In the last two columns of Table 2 we give the total number of TSOP faults detected by the proposed Boolean tests by adding those reported in Tables 1 and 2 and the percentage of faults detected out of the detectable faults constituting set of faults *F'*. From Table 2 we note that several TSOP faults whose detection requires Type-2 2-cycle transient faults can be detected by Boolean tests with 3 or more cycles.

Next we analyzed the TSOP faults not detected by Boolean tests but may be detected by Type-1 transient tests whose numbers are given in the last column of Table 1. The results of this analysis are given Table 3. First, we count the number of NAND and NOR gates containing the undetected TSOP faults. This number is given in column under # *Gates Including Undet. TSOP Faults*. Next, we check if each gate output stuck-at control value (which is 1 for NAND and 0 for NOR gates, respectively) is redundant and the number of such redundant faults is given in column under # *Redundant Gate Output Stuck-at Controlled Value*. The redundant stuck-at faults are classified into two groups, unable to activate the fault site and unable to propagate the fault effect. We note that redundant stuck-at faults always exist in the circuits including undetected TSOP faults and the majority of redundant stuck-at faults are due to unable to activate the fault sites. The number of TSOP faults inside the gates with redundant output stuck-at faults is given in the last column of Table 3. One can note that significant number of TSOP faults undetected by Boolean tests exists in the redundant logic in s38584. The TSOP faults detectable by transient tests, if present, may impact circuit's normal operation when they are presented. Since replacing the redundant gates by a constant will not change circuit function and the validation of transient tests is timing dependent, it is desirable to remove the redundant gates to avoid the TSOP faults inside the redundant gates causing unnecessary yield loss or field returns. It should be noted that the above mentioned potential circuit malfunction due to undetectable TSOP faults is different than what has been observed in the case of redundant stuck-at faults which when present may invalidate tests in a test set that detect all detectable faults or causes some originally redundant faults becoming detectable. Thus in the case of stuck-at faults the concern is malfunction due to additional fault(s) beyond the occurrence of the first stuck-at fault at a redundant site.

5. Conclusions

Detection of transistor stuck-open (TSOP) faults in CMOS logic circuits was investigated with the objective of developing methods to generate tests that are based on steady state Boolean analysis of circuits under test. Results on the larger ISCAS-89 circuits showed that Boolean tests achieve TSOP fault coverage of over 99%. Many of the TSOP faults not detected by Boolean tests are associated with redundant gates which can be removed from the circuits without effecting their functionality.

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