Modeling CMOS Gates Using Equivalent Inverters

Spyridon Nikolaidis
Department of Physics
Aristotle University of Thessaloniki
Thessaloniki, Greece
snikolaid@physics.auth.gr

***Abstract*—In this paper a complete approach for timing and power modeling and characterization of the CMOS gates is proposed. At first, a simplified but still accurate transistor current model is proposed taking into account the nanoscale effects which have a countable effect on the circuit behavior. Using the expressions of the transistor current, the differential equation which describes the operation of the CMOS inverter is solved analytically and expressions for the output voltage and supply current and thus for propagation delay and the power consumption are derived. These expressions are parametric according the input signal slew, output load, transistor widths, supply voltage, temperature and process. Complex gates are replaced by equivalent inverters with similar behavior and the expressions developed for the inverter are employed. Parametric expressions are derived for the transistor widths of the equivalent inverters using a fitting procedure. Results for the NAND and NOR gates show that the proposed approach presents a sufficient accuracy with an average error in propagation delay at 5%.**

Keywords—CMOS gate modeling; Inverter modeling; Equivalent inverter; Transistor current model; Timing-power model.

I. INTRODUCTION

Timing and power modeling of the CMOS gates is a very important task in the IC market since it eliminates costly iterations in the manufacturing procedure. Characterization of the gates based on accurate timing and power consumption models, permits us in making predictions for the circuit behavior early in the design phase. In this way, the required specifications are ensured before construction.

Current based models are preferred by industry for timing and power characterization of the CMOS gates. This is the case of the Composite Current source (CCS) technology [1] used by Synopsys. Based on a pre-characterization phase the waveforms of the supply and output currents for all the design corners, captured by simulation, are stored and used for making predictions for the propagation delay, output voltage slew and power consumption. Because of the required simulation this approach is accurate (error about 2% regarding BSIM) but slow and also needs the time consuming manipulation of large files.

Analytical models, on the other side, can provide similar predictions but much faster sacrificing some accuracy. A few approaches have been proposed for this case. These are based on the analysis of the operation of the gates to result in analytical formulas for the circuit characteristics like propagation delay, power consumption, etc. However, the direct analysis of the CMOS gate is a cumbersome problem much complicated by the nanoscale effects raised in the current technologies. Thus, the approach mostly proposed by the researchers is the use of an equivalent inverter to model the complex behavior of the CMOS gate. According to this method, analytical expressions are developed first for the CMOS inverter. Then, every gate is replaced by an equivalent inverter, by defining appropriate sizes for the transistors of the inverter, so that it can provide a similar behavior to that of the gate. Finally, the expressions, derived for the CMOS inverter, are used on the equivalent inverter to provide predictions for the gate's characteristics.

Some methods have been proposed in the past for direct analysis of the transistor structures to calculate the appropriate sizes of the transistors of the equivalent inverter [2-3]. However, they are based on assumptions for the relative operation of the transistors which are not further valid in the nanoscale regime. The application of these methods to current technologies leads to significant errors making their use inappropriate.

The proposed approach starts with the development of a simplified transistor current model. This model incorporates the main nanoscale effects which present a significant impact in the behavior of the circuits. The expressions for the transistor current are used for solving the differential equation which describes the operation of the CMOS inverter. Analytical expressions are developed for the output voltage waveform, the supply current, the propagation delay and the output waveform slew of the inverter. These expressions are fully parametric regarding input signal slew, τ, output load, C_{out}, transistor widths, W, supply voltage, V_{DD}, and temperature, T.

The transistor sizes of the equivalent inverter are calculating by a fitting procedure based on HSPICE simulations. For all the design corners, defined for the used library, and for different values of of W, V_{DD} and T a number of simulations are performed. The widths of the transistors of the equivalent inverter are selected so that it can provide a

978-1-4799-6780-3/15 $31.00 © 2015 IEEE
DOI 10.1109/DDECS.2015.20

similar output voltage waveform with that of the gate it substitutes. Using a fitting procedure, parametric expressions for the transistor widths are produced. The values for the transistor widths, calculated by this way, are by far more accurate than an alternative analytical method can offer. So, by this study the limits of the equivalent inverter approach are determined. As a case study the industrial oriented NangateOpenCellLibrary [4] for the 45nm PTM technology [5] is used.

II. Transistor Current Model

The proposed approach of modeling CMOS gates is based on solving the differential equation which describes the operation of the CMOS inverter. Simplified but still accurate expressions for the transistor currents has to be developed, so that the differential equation to can be solved analytically. For this reason, a modification of the transistor drain current model presented in [6] is used including analytical expressions for the threshold voltage V_t and the DIBL factor η_{DIBL}. To increase the accuracy in the analysis of the inverter, the subthreshold transistor current is taken into account since it has a considerable value in nanoscale technologies. Furthermore, in order the proposed gate model to be parametric regarding temperature, the transistor current model has been extended to include its dependence on temperature. A first version of this model has been presented in [7].

III. Modeling the CMOS inverter

The CMOS inverter is the basic structure of the digital circuits. In general, a complex CMOS gate consists of a NMOS and a PMOS transistor structures and depending on the values of the inputs its output voltage changes value from 0 to 1 or 1 to 0. The current through these structures, for a given process, depends on the way the transistors are connected, the applied input signals, the width of the transistors, the supply voltage and temperature. Defining an appropriate width for a single transistor it could provide a similar current waveform to that of the structure. An equivalent inverter could be constructed by using transistors with appropriate widths to provide a similar behavior to that of a complex gate. This makes the analysis of the inverter a major task in EDA market.

The CMOS inverter is shown in Fig. 1. The parasitic capacitances which have a significant impact on the behavior of the inverter are also shown. C_m is the coupling capacitance between input and output node, corresponding to gate-to-drain capacitance of both transistors. C_{db} corresponds to drain-to-bulk capacitance while C_{out} corresponds to output load capacitance.

Analysis of the operation of a circuit means finding the voltage and current waveforms at any node and branch of the circuit. In the case of the inverter there is only one node, the output node. If the voltage waveform on this node is determined, then the currents through all the branches (transistors and capacitances) can also be determined.

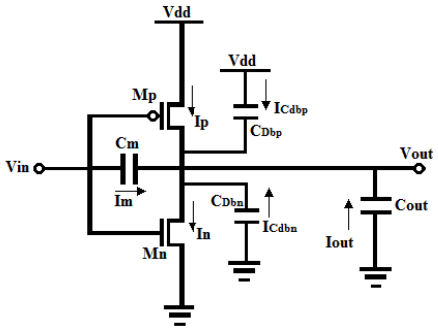

Fig .1. The CMOS inverter

The operation of the inverter is described by the differential equation resulted by applying the Kirchhoff's current law at the output node:

$$I_n + C_{dbn}\frac{dV_{out}}{dt} = I_p - C_{out}\frac{dV_{out}}{dt} + C_m\left(\frac{dV_{in}}{dt} - \frac{dV_{out}}{dt}\right) - C_{dbp}\frac{dV_{out}}{dt} \qquad (1)$$

where the transistor currents, I_n and I_p, are replaced by their expressions. As an input, a rising or falling ramp is applied. Appropriate average values according to the transistor operation mode are determined for the parasitic capacitances using HSPICE simulations.

The differential equation has to be solved during whole the time the output is in transition, which starts at the starting time of the input ramp signal. During this time interval, transistors operate in various modes and the combination of these modes (also with the input state) defines the different regions of operation. The structure of the solution flow for a rising input ramp has been presented in [7]. A similar flow for the falling input ramp exists. The differential equation has to be solved for every region of operation. To do that, some reasonable assumptions have been adopted [7-8]. Finally, a parametric expression for the output voltage according to the input transition time, output load, transistor width, supply voltage and temperature is derived. Table I shows the design corners defined by the used library and the range of the values of the parameters.

TABLE I. Parameter corners and ranges

Input slew, τ *(ps)*	2.9, 12, 43, 102, 195, 325, 496
Load capacitance, C_{out} (fF)	0.37, 1.9, 3.8, 7.6, 15.1, 30.3, 60.6
NMOS transistor width, W_n *(nm),* (range)	90 - 400
Supply voltage, V_{DD} (V), (range)	0.7 - 1.25
Temperature, T (°C), (range)	0 - 125

Using the expression of the output voltage, the expression of the output current through C_{out} results as $I_{out} = C_{out}\, dV_{out}/dt$. The current from the supply voltage can be calculated by

$$I_{Vdd} = I_P \pm C_{gsp}\frac{dV_{in}}{dt} - C_{dbp}\frac{dV_{out}}{dt} \qquad (2)$$

where "+" or "-" are used for the case of falling or rising inputs, respectively, while C_{gs} is the gate-to-source capacitance. A corresponding equation can be derived for the ground current.

The NangateOpenCellLibrary [4] for the PTM 45nm technology [5] is employed. Fig. 2 shows a comparison of the proposed model with HSPICE for an output voltage waveform for a rising input and V_{DD}=1.1V, T=25°C, τ=195.25ps, C_{out}= 15.18fF and W_n=250nm. In Fig. 3 a comparison for the supply current for the falling input case is presented. The accuracy of the proposed model is obvious.

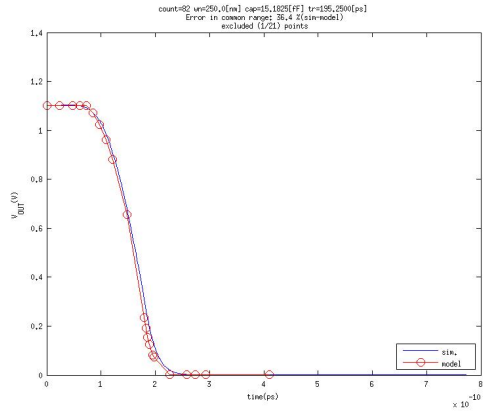

Fig. 2 Output voltage comparison for a CMOS inverter and for rising input

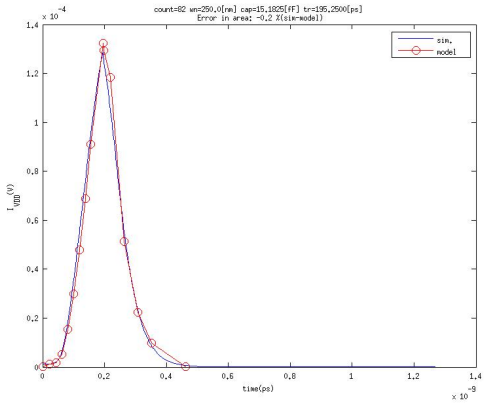

Fig. 3 Supply current comparison for a CMOS inverter and for falling input

Expressions for the propagation delay are also provided. Regarding propagation delay, an average error of 3% with a maximum less than 10% is presented in all the corners for the typical case (V_{DD}=1V, T=25°C). For T=25°C and in whole the range of the V_{DD} (0.7V-1.25V) the average error increases to 4.5% while for different values of T the error is about 8%.

IV. THE EQUIVALENT INVERTER APPROACH

The analysis of the inverter towards an analytical solution is a complex procedure. This prevents a complete analysis of the complex gate. Instead, the approach of the equivalent inverter provides sufficient results. According this, the NMOS and PMOS transistor structures of a gate are replaced by single NMOS and PMOS transistors which provide similar current waveforms under similar bias conditions. By this way, an equivalent inverter provides a similar output voltage waveform as the gate it replaces.

The problem is to estimate the appropriate widths to emulate the operation of the transistor structures. Some methods have been proposed in the past [2-3], but they are based on assumptions which are not further valid for nanoscale technologies, mainly because of the significant impact of the channel length modulation effect on the transistor current values. The application of such methods in current technologies leads to significant and unacceptable errors.

The effectiveness and the accuracy of the approach of the equivalent inverter are studied here. The widths of the transistors of the equivalent inverter are calculated based on HSPICE simulations. For all the design corners and the ranges of the parameters the output waveform of the gate is captured by simulation. Then the appropriate width of the transistors of the equivalent inverter is determined so that it provides a similar output waveform with that of the gate. In this way, the transistor width of the equivalent inverter is determined as a function of the input transition time, the output load, the width of the transistors of the gate, the supply voltage and the temperature. By applying a fitting procedure, the precise functions of the appropriate widths are defined [9]. It should be mentioned that the output load in the equivalent inverter has to slightly be increased to include the impact of the parasitic capacitance of the extra transistor area of the gate.

In Fig. 4 the output voltage waveform of the NAND gate for a rising input to the bottom transistor (the other is "1") is compared to that of the equivalent inverter. The width of the equivalent transistor is calculated by the derived expressions. This is for V_{DD}=1.1V, T=25°C, τ=102.5ps, C_{out}= 7.59fF and W_n=400nm. In Fig. 5 a comparison for the ground current waveform is also presented.

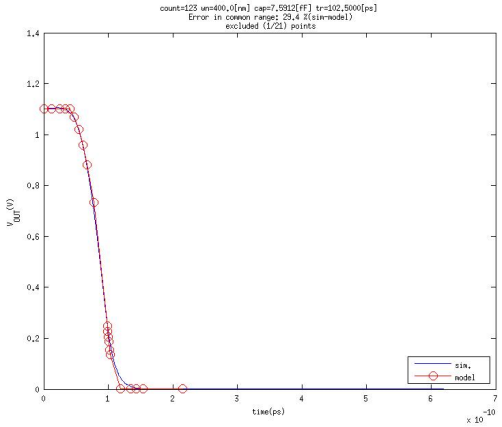

Fig. 4 Output voltage comparison for a NAND gate and for a rising input

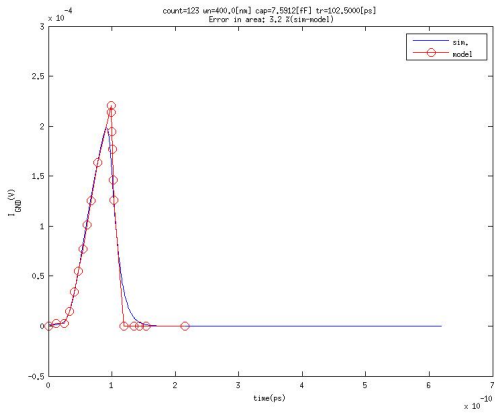

Fig. 5 Ground current comparison for a NAND gate and for a rising input

The accuracy is obvious. Regarding propagation delay, the error for the typical case is about 5%. Some results regarding the propagation delay of the NOR and NAND are provided in Table II.

V. Conclusions

The approach of using equivalent inverters for modeling complex CMOS gates is investigated. An inverter model is developed by solving analytically the differential equation which describes its operation. To do that, a simplified but still accurate transistor current model is proposed. In this way, analytical expressions can be derived for the voltage and current waveforms, as well as the propagation delay and the power consumption accelerating the characterization procedure. These expressions are parametric according the input signal slew, the output capacitive load, the transistor width, the supply voltage and the temperature. An average error of about 5% has been determined for the estimation of the propagation delay in CMOS gates.

Acknowledgment

This work was supported by Hellenic Funds and by the European Regional Development Fund (ERDF) under the Hellenic National Strategic Reference Framework (ESPA) 2007-2013, according to Contract no. 11ΣΥΝ_5_719 project NANOTRIM.

References

[1] CCS Timing, Technical White Paper, Version 2, Synopsys, Inc., Dec. 2006, http://www.opensourceliberty.org/ccspaper/ccs_timing_wp.pdf

[2] Kabbani, A., "Complex CMOS gate collapsing technique and its application to transient time," Journal of Circuits, Systems and Computers 19 (5), pp. 1025-1040, 2010.

[3] A. Chatzigeorgiou, S. Nikolaidis, I. Tsoukalas, "A Modeling Technique for CMOS Gates," IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems, Vol. 18, No 5, pp.557-575, May 1999.

[4] Nangate 45 nm Open Cell Library, Version 1.3, Nangate Inc., Jul. 2009. [Online]. Available: http:// www.si2.org/openeda.si2.org/projects/nangatelib.

[5] Predictive Technology Model (PTM), http://www.eas.asu.edu/ptm/

[6] E. Consoli, G. Giustolisi, G. Palumbo, "An accurate ultra-compact I-V model for nanometer MOS transistors with applications on digital circuits," IEEE Trans. Circuits Syst., vol. 59, no. 1, Jan. 2012.

[7] P. Chaourani, I. Messaris, N. Fasarakis, M. Ntogramatzi, S. Goudos, S. Nikolaidis, "An Analytical Model for the CMOS Inverter," International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS), Palma De Mallorca, Spain, 2014.

[8] P. Chaourani, S. Nikolaidis, "A unified CMOS inverter model for planar and FinFET nanoscale technologies," 17th Symposium on Design & Diagnostics of Electronic Circuits & Systems, Warsaw, Poland, 23-25 April, 2014.

[9] Ch. Galani, A. Tsormpatzoglou, P. Chaourani, I. Messaris, S. Nikolaidis, "A study for replacing CMOS gates by equivalent inverters," International Symposium on Circuits and Systems (ISCAS), Lisbon, Portugal, 2015.

TABLE II Propagation delay approximation for the NOR and NAND and for input applied at the closest to the power rail transistor

NOR (V_{DD} = 1V)															
T=25°C (rising)								T=125°C (falling)							
W(nm)	C_{out}(fF)	τ=10ps			τ=100ps			W(nm)	C_{out}(fF)	τ=10ps			τ=100ps		
		Delay (Model)	Delay (HSPICE)	Error (%)	Delay (Model)	Delay (HSPICE)	Error (%)			Delay (Model)	Delay (HSPICE)	Error (%)	Delay (Model)	Delay (HSPICE)	Error (%)
100	0.5	11.37ps	11.74ps	3.15	33.81ps	34.25ps	1.28	100	0.5	54.8ps	49.53ps	10.64	66.04ps	63.89ps	3.37
	15	144.8ps	145.2ps	0.28	169ps	169.5ps	0.29		15	815.2ps	792.8ps	2.83	818.6ps	806ps	1.56
400	0.5	7.676ps	7.985ps	3.87	25.69ps	26.13ps	1.68	400	0.5	28.57ps	28.45ps	0.42	44.24ps	44.4ps	0.36
	15	38.99ps	39.42ps	1.09	64.81ps	65.26ps	0.69		15	198.9ps	208.5ps	4.60	212ps	220.3ps	3.77
NAND (V_{DD} = 0.7V)															
T=25°C (rising)								T=125°C (falling)							
W(nm)	C_{out}(fF)	τ=10ps			τ=100ps			W(nm)	C_{out}(fF)	τ=10ps			τ=100ps		
		Delay (Model)	Delay (HSPICE)	Error (%)	Delay (Model)	Delay (HSPICE)	Error (%)			Delay (Model)	Delay (HSPICE)	Error (%)	Delay (Model)	Delay (HSPICE)	Error (%)
100	0.5	21.04ps	20.52ps	2.53	43.23ps	42.77ps	1.08	100	0.5	43.62ps	43.64ps	0.05	64.9ps	64.65ps	0.39
	15	290ps	276.3ps	4.96	295.5ps	298.1ps	0.87		15	633.9ps	633.6ps	0.05	678.5ps	678.3ps	0.03
400	0.5	12.84ps	13.43ps	4.39	33.1ps	32.52ps	1.78	400	0.5	26.02ps	26.03ps	0.04	50.05ps	49.67ps	0.77
	15	72.7ps	74.04ps	1.81	93.85ps	96.6ps	2.85		15	170.9ps	170.8ps	0.06	190.9ps	191ps	0.05