Reducing RMS Noise in CMOS dynamic reconfigurable latched comparator in 50 nm

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Abstract **This paper presents a new dynamic reconfigurable CMOS latched comparator that demonstrates low RMS noise, low offset and high gain. In this dynamic comparator circuit we make an independent inputs transistor and its input inverter circuit PMOS connected to clk1 with tail transistor. The proposed comparator circuit shows better RMS noise response i.e. 704.38μV as compare to previous comparator circuit i.e. 1.1208mV and better output driving capacity as compare to conventional comparator circuit. The proposed comparator is simulated and implemented in LT SPICE 50nm technology.**

Keywords— ***CMOS Comparator, RMS Noise, amplifier, LT SPICE***

I. INTRODUCTION

Operational amplifier is most abundant circuit used in electronic world and second circuit is Comparator. Comparator is a circuit that convert analogy signal into digital form. We can also say that comparator circuit is a single bit analog to digital convertor. This circuit is very attractive for high speed ADCs, data receiver and memory sense amplifiers (SAs). For fast speed and zero static power consumption, single stage comparator [4] is widely used. But in this comparator the input transistor overdrive voltage is limited, due to the addition of latch function with the input stage and which increase the number of transistors from supply voltage to ground. As a result the saturation period of the input transistors are restricted and noise is increases. Nowadays a two stage dynamic comparators [5] are used to suppress the noise presented in the dynamic comparator. In paper [1,2] presented a comparator, it has only one tail transistor which limit the current flowing through both output branches that is totally dependent on input difference ΔVin. To avoid this drawback,

Comparator circuit is divvied into input gain stage and output latch stage [3]. In this comparator circuit we required Clk and Clkb signals fir its operation. In this comparator we required high accuracy clock signal because second stage detect the voltage difference between first stage differential outputs. The high accuracy signal is achieved by a using the inverter circuit between both clock signal at the cost of increase clock loading that drive large PMOS transistor for small delay [5]. As a result the comparator load is increased and speed is degraded. in this comparator circuit if clk is leading the clkb then delay of the comparator is increase and speed is decreases. If the clk is lagging than clkb then power dissipation is increases. Clock skew problem is resolved in paper [5] by dividing large PMOS transistor in two PMOS transistors. This improvement is achieved at the cost of increased delay and noise performance. In paper [6] proposed a two stage comparator by which we can improve the noise performance. With the help of PMOS output latch proposed in [6] reduces the driving current at load stage and limits the saturation period of the input transistors. Low offset and low noise are the critical concern for comparator circuit for ADCs purpose. Inserting unbalance capacitance [4] at comparator output stage or adding an extra input pair transistors in comparator [5] circuit. As a result, the offset voltage is reduces but speed of the comparator is degraded. And another drawback of addition of an extra input pair transistor [5] or inserting unbalance capacitance [4] at comparator output stage is the complexity and area of the comparator is increases. In paper [7] presented a reconfigurable dynamic comparator circuit. In this comparator two different clock signals are used for minimizing the noise and inverter input stage. Due to inverter input stage, ti's nodes charging depends on the input signals applied in comparator circuit and the charging rate is affected.

In this paper we are proposed a new reconfigurable dynamic latched by which dependency of the input stage of ti's node is removed. This paper is organized as follows. Proposed Reconfigurable latched Comparator circuit and principle of operation in IInd section. In IIIrd section we compare the performance and RMS noise with previous work. IVth section provides Conclusion of the paper and References.

II. COMPARATOR ANALYSIS

A. Circuit Implementation

To avoid the noise performance in comparator circuit we required a large amplification at input stage or common input ΔVin. The gain of the dynamic amplifier is expressed as $g_m t/C$,

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(gm transconductance, t be time period for amplification and C be capacitive load) that keeps the input transistor in saturation region for giving time of amplification [8]. The two stage reconfigurable dynamic comparator [8] and proposed dynamic comparator architecture is shown in figure 1 and 2 respectively.

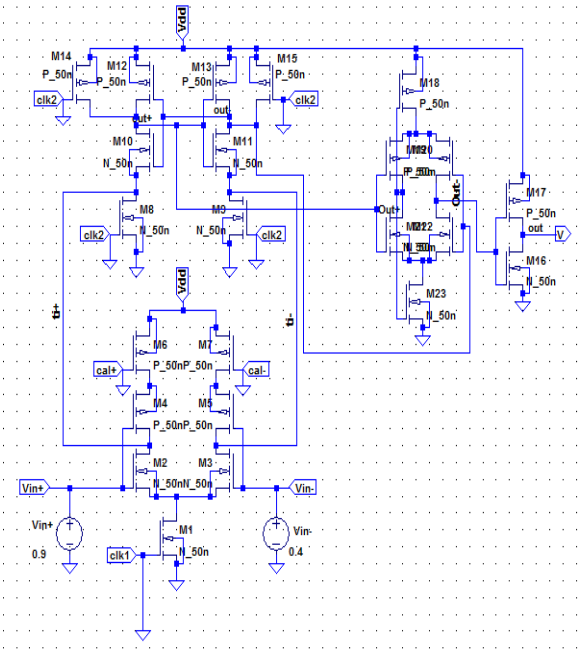

Fig. 1 Reconfigurable dynamic comparator

The comparator circuit is design and simulated with LT SPICE using 50nm cmosedu.medels_txt. The basic structural circuit of the proposed comparator from [5] and [8]. The input specification and clock frequency as Vdd = 1V, clock frequency = 3GHz, capacitive load = 7fF and temperature = 27˚C. The proposed dynamic comparator provides better RMS noise performance as compare to [7]. The total voltage gain and offset voltage is also improved in proposed dynamic comparator circuit.

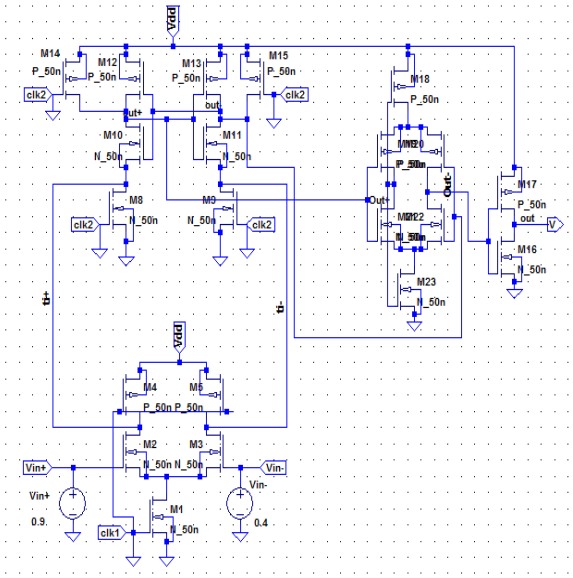

Fig. 2 proposed dynamic comparator

The proposed comparator operation principle, for reset phase (when clk1 and clk2 both are 0) transistor M4 and M5 continuously charge the ti's node to Vdd and M14 and M15 are charged output's node (out- & out+). For evaluation phase I (clk1 = 1 and clk2 = 0), in this case transistor M1 turns ON provided a current path and ti's nodes discharged from Vdd to ground. During this period M14 and M15 are still ON and provide current path for output's node (transistor M10 and M11).As a result the input transistors (M2 and M3) are in saturated mode. At evaluation phase II (clk1 = 1 & clk2 = Vdd), during this phase inverter pair (M10/M12 & M11/M13) and transistor M8 and M9 are turn ON. In this stage we regenerate the current difference from first stage to Vdd or ground at output's node.

B. Proposed Comparator Charecteristics

Due to the transistors M8 and M9 proposed comparator provide better noise performance and total voltage gain as compare to previous work. The DC response and transient response of the proposed comparator is shown in figure 2 and 3 respectively.

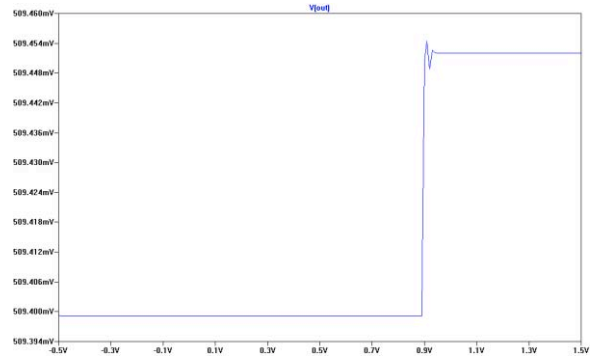

Fig 2 DC Response of proposed comparator

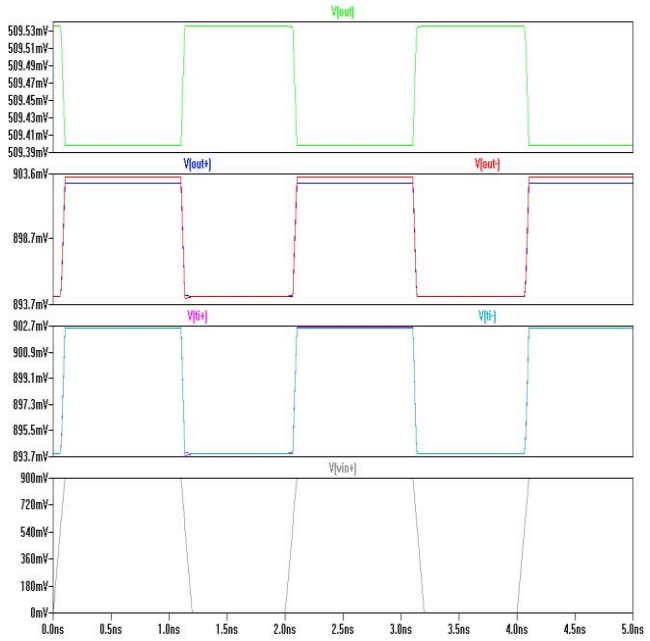

Fig. 3 Tran. Response of proposed comparator designations.

C. *Results*

The result of the proposed comparator circuit is calculated with the help of the LT SPICE simulation. The observed values of the proposed comparator circuit is

Vir = 0.080nS, Vif = 2.141nS and Vor = 0.627nS, Vof = 0.30nS.

Where,

Vir = Input rise voltage

Vif = Input Fall voltage

Vor = output rise voltage

Vof = output fall voltage.

(i) Offset Voltage = 509.399mV

(ii) Total voltage gain, Av = $\frac{VOH - VOL}{VIH - VIL}$ = 9.84 x 10^{-4}

(iii) Propagation Delay Time = $\frac{Rising\ propagation\ time - Falling\ propagation\ t}{2}$

= 0.65nS

(iv) Speed = 1.538GHz

(v) RMS Noise = 704.38µV

The calculated results of the proposed comparator are shows better response as compare to Chan and Zhu circuit [7].

III. COMPARISOIN OF PREVIOUS WORK

Table1 shows comparison result of proposed comparator with previous works:-

Table1. Result Comparison

Comparators	Transistor Count	Offset Voltage (mV)	Total Voltage Gain	Propagation Delay time (nS)	Speed (GHz)	RMS Noise
Dynamic latch based comparator	11	508.126	$5x10^{-4}$	0.758	1.319	1.843mV
Dynamic comparator without calibration	15	526.602	$6.72x10^{-4}$	0.730	1.3698	4.495mV
Reconfigurable dynamic latch comparator	15	509.544	$4.83x10^{-4}$	0.735	1.3605	1.1208 mV
Proposed dynamic comparator	13	509.399	$5.84x10^{-4}$	0.650	1.5380	704.38 µV

All the results are calculated on LT SPICE models simulation software in 50nm technology. RMS noise of different comparators are compared and shown in figure 4.

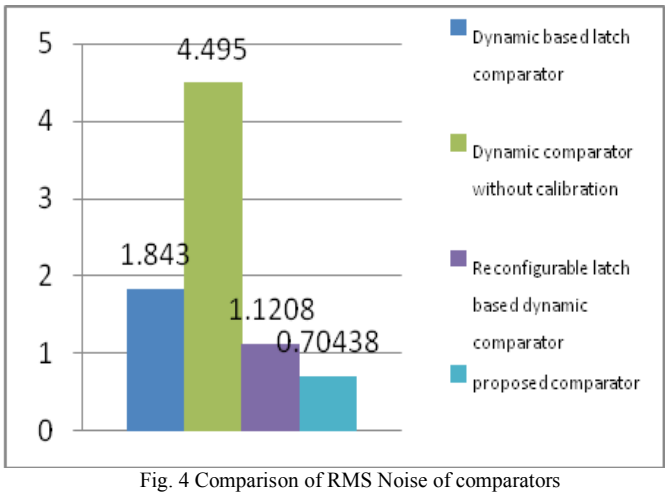

Fig. 4 Comparison of RMS Noise of comparators

IV. CONCLUSION

With the help of this paper, we developed a new dynamic reconfigurable comparator circuit. This proposed comparator circuit reducing the RMS noise i.e. 704.38µV and improved the speed due to reduction of propagation delay by connecting the M4 and M5 transistors to clock signal. The clock signal clk2 is connected to transistor M8 and M9 that limited the saturation time period of input transistor and due to that ti's node discharge totally dependent on inputs difference. The comparisons of all parameters are shown in the table 1. Reduction of RMS noise and propagation delay in the proposed comparator is obtained at the cost of clock loading.

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