Design and Implementation of a Reversible Central Processing Unit

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***Abstract*—This work addresses the reversible circuit design using novel modularization approach by presenting architecture of a logically reversible processor based on the Von Neumann architecture that can operate with very low power consumption, protection of power analysis attack and long span of life due to less heat dissipation. The organization and architecture of the proposed processor is designed from scratch. Sequential algorithms are proposed to produce the components of the reversible processor. The capabilities of the new processor is determined, the datapath layout is designed to handle the necessary capabilities, the instruction format is defined and the necessary logic is also constructed to control the datapath. To estimate the execution time of the algorithm, we consider the computational complexity, memory access patterns and the complexity of the instructions. Existing component designs are compared with the proposed components and theorems and lemmas are presented to prove the superiority of the proposed architecture. The proposed design is simulated and the simulation result verifies the correctness of the proposed design.**

***Index Terms*—Reversible Logic, Reversible CPU, Quantum Cost, Garbage Output.**

I. Introduction

Power crisis is a vital problem in today's world. In recent years, the growing market of electronic systems suffers from power dissipation and heat removal problem. If more and more power is dissipated, system becomes overheated which reduces the life time of the electronic system. The need of micro-electronic circuits with low power dissipation leads to the implementation of reversible logic circuit. Bennett [1] proved that the one-to-one mapping between the inputs and outputs of reversible circuit drastically reduces the power consumption and heat dissipation of a circuit. Today security in digital computing and communications is of prime importance and therefore cryptographic protocols play a major role.

David [2] proved that reversibility plays a vital role in quantum computation. Quantum gates and reversible logic gates are closely related to each other. Like classical reversible circuits, the number of input quantum bits must be equal to the number of output quantum bits. The quantum gates and circuits must be reversible. So, the quantum circuits can directly be designed from reversible circuits.

Processor design is indeed a difficult task and thinking the organization and architecture of the design in reversible way requires a lot of works. The irreversible processors dissipate a significant amount of heat and they require more power than the corresponding reversible one. A reversible processor can overcome these problems. As reversible computing is a new era, very few works [3], [4] regarding reversible processor have been done. As well as, there is no established patent work in this area. The existing reversible processor architectures [3], [4] lack rigor and completeness. These parameters motivate this work of reversible processor design. In this work, we present a logical reversible processor design architecture and algorithms that try to fill up the gap between realization of the reversible architecture and completeness of the design.

II. Basic Definitions

In this section, we present the basic definitions regarding reversible logic.

A. Reversible Gate

Reversible gate is an n-input and n-output (denoted by $n \times n$) circuit that produces a unique output pattern for each possible input pattern. In other words, reversible gates are circuits in which the number of outputs is equal to the number of inputs and there is a one-to-one correspondence between the vector of inputs and outputs.

B. Garbage Output

Unwanted or unused output of a reversible gate (or circuit) is known as ***garbage output***, i.e., the output(s) which is(are) needed only to maintain the reversibility is (are) known as garbage output(s).

C. Quantum Cost

The ***quantum cost*** can be derived by substituting the reversible gates of a circuit by a cascade of elementary quantum gates [5]. Elementary quantum gates realize quantum circuits that are inherently reversible and manipulate qubits rather than pure logic values. The state of a qubit for two pure logic states can be expressed as $|\psi> = \alpha| 0 > + \beta| 1 >$, where $| 0 >$ and $| 1 >$ denote 0 and 1, respectively, and and α and β are complex numbers such that $| \alpha |^2 + | \beta |^2 = 1$. The most used elementary quantum gates are the NOT gate, the controlled-NOT (CNOT) gate, the controlled-V gate and the controlled-V+ gate.

III. Proposed Work

The internal arrangement of a microprocessor varies depending on the design and the intended purposes of the microprocessor. A microprocessor includes an arithmetic logic unit (ALU) and a control unit (CU) section. These two sections are connected to memory and I/O by buses which

978-1-4799-8719-1/15 $31.00 © 2015 IEEE
DOI 10.1109/ISVLSI.2015.74

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carry information and signal between the units. They have a defined datapath. The ALU performs the arithmetic and logical operations. The control logic section retrieves instruction operation codes from memory, and initiates whatever sequence of operations of the ALU requires to carry out the instruction. A single operation code affects many individual datapaths, registers, and other elements of the processor. Following steps are considered to design the desired reversible central processing unit (CPU):

- Design the overall structure of the reversible CPU.
- Layout the datapath to handle all of the operations of the reversible CPU.
- Design the reversible realizations of the flip-flops.
- Design the reversible memory circuits (such as buffer registers and counter circuits) using the proposed reversible flip-flops of the previous step.
- Design the arithmetic circuits such as adder, multiplier, divider, comparator etc.
- Design the reversible realization of ALU.
- Design the reversible control unit of the processor by designing an efficient instruction decoder.
- Construct the necessary logic to control the datapath.
- Realize the overall architecture and organization of the proposed reversible processor.
- Analysis of the proposed reversible central processing unit in terms of cost and performance efficiency.
- Simulate the design using Microwind DSCH 3.5 [6] and CMOS 45 nm Open Cell Library [7] software.

The architecture of the proposed reversible processor is shown in Fig. 1.

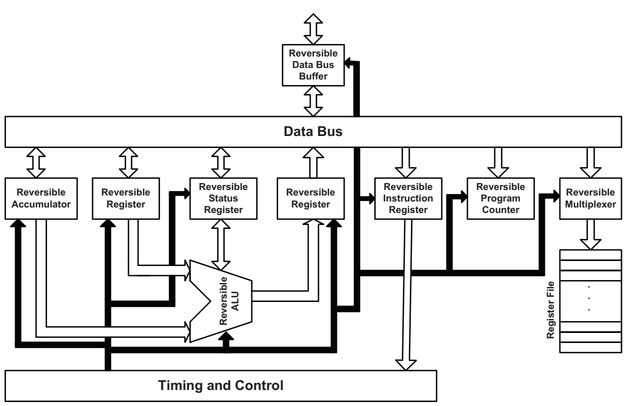

Fig. 1. Outline of the Design of the Proposed Reversible Processor

The datapath of the proposed reversible processor is shown in Fig. 2. The control signals are not shown in the diagram for simplicity.

According to the block diagram and the datapath design the proposed reversible processor has been divided into small components. The reversible realization of the proposed components are discussed in the following subsections.

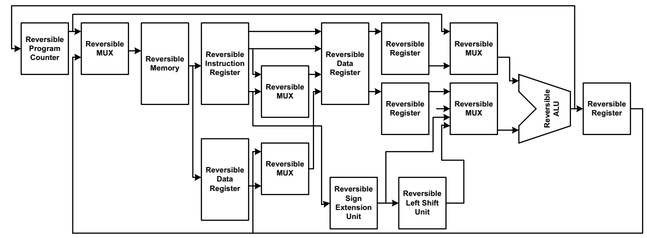

Fig. 2. Datapath Design of the Proposed Reversible Processor

A. Proposed Reversible Memory Components

Flip-flops (FF) are the basic elements of a register. We use template matching algorithm to propose a reversible J-K FF with minimum quantum cost. This J-K FF is used to design the instruction register. We propose a new reversible gate, namely BJ gate [8], to design a reversible J-K FF. The proposed reversible J-K FF requires only one gate, it produces only one garbage output and it has 12 quantum cost. The design of the proposed J-K FF is shown in Fig. 3.

The proposed reversible J-K FF achieves the improvement of 66.6% in terms of number of gates, 66.6% in terms of garbage outputs, 66.6% in terms of delay and 4.28% in terms of quantum cost over the existing best one [9].

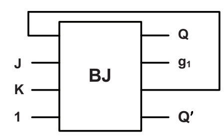

Fig. 3. Proposed Reversible J-K Flip-Flop

This proposed J-K FF is used to design the registers. A reversible 16-bit register can be designed using sixteen HNFG gates and sixteen proposed J-K FFs. The J-K FFs take the inputs through HNFG gates and with the change of the clock pulse they produce the normal and complemented outputs.

The sequence counter is also designed using four proposed J-K FFs and four Feynman gates. The J-K FFs change states with the positive clock edge and the counter counts from 0 to 15. This optimized design of sequence counter produces 4 garbage outputs.

B. Proposed Reversible Multiplexer

Reversible Multiplexer (Mux) is required to select a certain input from various input sources. A reversible 4-to-1 mux is designed with Fredkin gates. The proposed design of 4-to-1 mux is shown in Fig. 4. The proposed reversible 4-to-1 mux achieves the improvement of 57.14% in terms of number of gates, 54.54% in terms of garbage outputs, 73.68% in terms of quantum cost and 57.14% in terms of delay over the existing best one [10].

C. Proposed Reversible Decoder

The control unit requires decoders to decode the instructions. We propose the design of an n-to-2^n decoder. To design

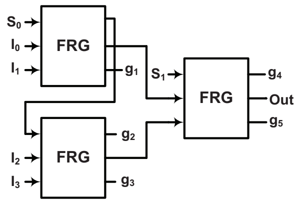

Fig. 4. Proposed Reversible 4-to-1 Multiplexer

this decoder at first we propose a reversible 2-to-4 decoder which was used to construct a 3-to-8 decoder and so on. The design of an improved 2-to-4 decoder was very challenging as an existing 2-to-4 decoder [11] requires only one gate and it does not produce any garbage outputs. So, there was no scope to improve gate count, garbage outputs and delay. Exhaustive search was used to find the reversible gate with optimal solution which produces the minimum quantum cost. We propose a new reversible gate, namely HL gate [8] to design a 2-to-4 decoder. The proposed 2-to-4 decoder requires only one gate without any garbage output which has 7 quantum cost. Our proposed design has the same gate count, garbage outputs and delay. But it has improved quantum cost. A reversible 3-to-8 decoder can be designed using one 2-to-4 reversible decoder and four Fredkin gates. The achievement of the design of 3-to-8 design was greater as the existing best 3-to-8 decoder [12] is not much optimized. The designs of the proposed reversible 2-to-4 decoder and 3-to-8 decoder are shown in Fig. 5(a) and Fig. 5(b) respectively.

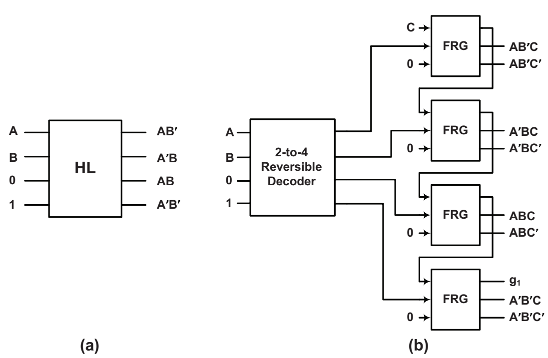

Fig. 5. Proposed Reversible (a) 2-to-4 Decoder (b) 3-to-8 Decoder

D. Proposed Reversible Control Unit

A control unit is a circuit that directs operations within the computer's processor by directing the input and output of a computer system. The control unit consists of two decoders, a sequence counter, and a number of control logic gates. It fetches the instruction from instruction register. The inputs to the control logic gates come from two decoders, flip-flop and instruction register. The outputs of the control logic circuit are: signals to control the inputs of the registers, signals to control the read and write inputs of memory and signals to set, clear or complement the flip-flops.

A step by step design technique has been proposed to design the control unit which connects all the proposed components with some other extra circuitry. The block diagram of the proposed control unit is shown in Fig. 6.

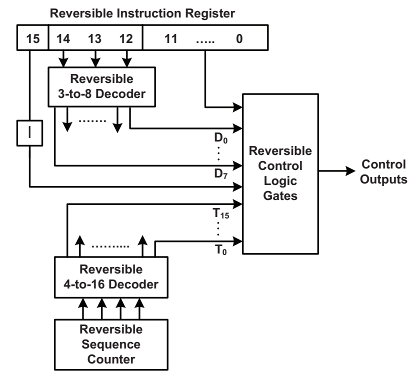

Fig. 6. Proposed Reversible Control Unit

E. Proposed Reversible Comparator

A magnitude comparator takes two numbers as input in binary form and determines whether one number is greater than, less than or equal to the other number. Comparators are used in central processing unit. We propose a compact and improved algorithm for constructing a compact reversible n-bit binary comparator circuit. In order to improve the design, we use quantum cost minimization algorithm to design an n-bit comparator. Reduction rules and algorithms are applied by template matching to minimize the quantum cost. The whole comparator is divided into three modules. They are as follows: We propose an MSB comparator circuit for comparing the nth bit (MSB) of two n-bit numbers. Then, a single-bit GE (greater or equal) comparator cell has been designed to generate greater and equal signal for the remaining (n-1) bits of two numbers with the previous comparison result of MSB. A single-bit LT (less than) comparator cell is designed to determine the less than signal. These three components with minimum quantum cost are then cascaded with each other using efficient techniques to design 2-bit and n-bit reversible binary comparators more compactly. A reversible 2-bit binary comparator consists of a proposed reversible MSB comparator, a single-bit GE comparator and a single-bit LT comparator circuit. The reversible design of 2-bit binary comparator is shown in Fig. 7. The detail design of the individual blocks are not shown here due to space constraints.

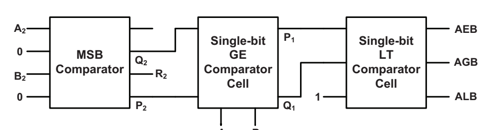

Fig. 7. Proposed Reversible 2-bit comparator

The proposed reversible 64-bit comparator achieves the improvement of 24.4% in terms of number of gates, 19.9%

in terms of garbage outputs, 7.7% in terms of quantum cost, 25.77% in terms of area and 3.43% in terms of power over the existing best one [13].

F. Proposed Reversible Multiplier

Multiplier circuit is used in a processor. Multiplier circuit mainly has two components: Partial Product Generation (PPG) circuit and the Multi-Operand Addition (MOA) circuit. A multiplier circuit can be optimized in two ways. The algorithm of the multiplication can be optimized, as well as, the construction procedure of the PPG circuit and MOA circuit can be optimized. Firstly, we construct efficient template using reversible gates to reduce the quantum cost and delay. Secondly, we use an efficient searching technique to find the appropriate positions of different components of the proposed circuit. Finally, we propose two efficient algorithms which produce high speed minimum cost PPG circuit and MOA circuit of the proposed multiplier.

The comparative study shows that the proposed reversible 4×4 multiplier achieves the improvement of 26.32% in terms of number of gates, 12.5% in terms of garbage outputs, 17% in terms of quantum cost and 20.97% in terms of constant inputs over the existing best one [14]. The proposed reversible $n \times n$ multiplier requires $n(2n-1)$ gates, $4n(n-1)+1$ garbage outputs and $17n(n-1)+1$ quantum cost; where as the best existing fault tolerant reversible multiplier [14] requires $n(2n-1)+\lfloor 5n/2 \rfloor$ gates, $2n(n-1)$ garbage outputs and $n(19n-17)+7+2\lfloor n/2 \rfloor$ quantum cost.

G. Proposed Reversible Divider

Divider circuit is used in a processor. We propose two design techniques to construct reversible n-bit floating point non-restoring division circuit. In the first approach of the reversible divider circuit, we propose carry propagate 2's complement adder and shifters. To speed up the division technique, we propose a major modification in the second approach of the reversible divider. We omit the carry propagation to avoid the propagation delay and introduce two new vectors and a single carry look-ahead adder circuit. Subtraction is implemented using 2's complement adder. Both of the approaches can handle floating point numbers. Exhaustive search method is used to find the appropriate positions of reversible gates to obtain the minimum cost parameters for a specific function that are used to design the reversible divider circuit more compactly. The comparative study shows that the proposed reversible conventional 4-bit divider achieves the improvement of 62.92% in terms of number of gates, 70.97% in terms of garbage outputs and 74.83% in terms of quantum cost over the existing best one [15]. The proposed reversible high speed 4-bit divider achieves the improvement of 22.47% in terms of number of gates, 17.74% in terms of garbage outputs and 43.87% in terms of quantum cost over the existing best one [15].

IV. Conclusions

In this work, reversible logic syntheses with the minimum cost factors are carried out for the components of the reversible processor. Many important contributions have been made in the literature towards the reversible implementations of arithmetic and logical structures; however, there have not been many efforts directed towards efficient approaches for designing reversible ALU (Arithmetic Logic Unit). Currently we are working on the design of the reversible ALU. We will propose an efficient approach to design the reversible ALU. Finally all the components of the reversible CPU (Central Processing Unit) will be interfaced together with necessary connecting circuits to get the complete reversible CPU. The proposed reversible CPU can make a significant contribution in the field of low power reversible computing and quantum computing.

Acknowledgment

This work was done under the assistance of Prime Minister's Research and Higher Studies Fund given by the Prime Minister's Office and ICT Innovation Fund given by the Ministry of ICT, Government of the People's Republic of Bangladesh.

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