Performance Comparison of Pass Transistor and CMOS Logic Configuration based De-Multiplexers

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***Abstract*—This research paper analyzes the performance of De-Multiplexer (De-Mux) using Pass Transistor Logic Configuration (PTLC) and CMOS Logic Configuration (CLC). Furthermore, a comparison between the performances of both the configurations in terms of power dissipation, chip area, power supply and drive current levels are analyzed. Besides this, paper also signifies more than 50% decrement in interconnect lengths, chip area and number of transistors count while using pass transistor logic configuration in comparison to 1:2 De-Mux implemented with CMOS logic configuration. Moreover, reduction in supply voltage and decrement in power dissipation up to 70% is observed in pass transistor logic comparing to CMOS logic.**

Keywords*— *CMOS logic configuration, De-multiplexer, Pass transistor logic, Power dissipation, Chip area.

I. INTRODUCTION

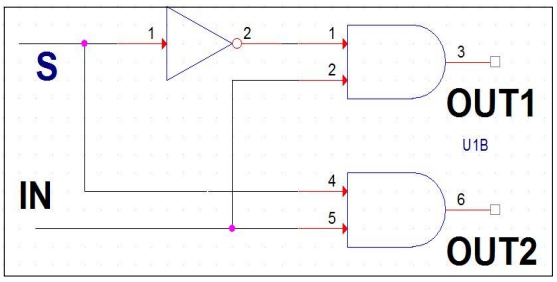
A de-multiplexer (De-Mux) is a combinational digital circuit that has one input and more than one output. It is used when a circuit wishes to send a signal to one of many devices [1]. In this paper, the effect of change in architecture of 1:2 de-multiplexer in terms of power dissipation, chip area, supply voltage and output current is analyzed. The schematic diagram and characteristic table for 1:2 de-multiplexer is shown in Fig. 1 (a) and (b), respectively. It is observed from the diagram that 1:2 de-multiplexer has one input line IN and one select line S, whereas, OUT1 and OUT2 are the two outputs. When S is in logic state 1 (high) output line OUT2 is selected and reflects input at terminal A. Similarly, when S is logic- 0 (low) output line OUT1 is selected and input at IN reaches output line OUT1. The 1:2 de-multiplexer logic is implemented using gate level configuration that includes two-logic gate and one inverter circuit [1]. The observed result indicates that the power dissipation, chip area, output current level and other parameters vary with change in transistor technology node or architecture.

This research paper analyses the behavior of 1:2 de-multiplexer in pass transistor logic and conventional CMOS logic architecture using ORCAD 16.6 simulation. The Technology node and supply voltages of 180nm and 1.8V are considered from experimental results respectively so that all architecture/configurational impact can be measured significantly with respect to different architectures. The results show that the 1:2 de-multiplexer logic implementation in pass transistor logic architecture perform better in comparison to CMOS logic configuration mainly in terms of area consumption, number of transistor counts, supply voltage and power dissipation.

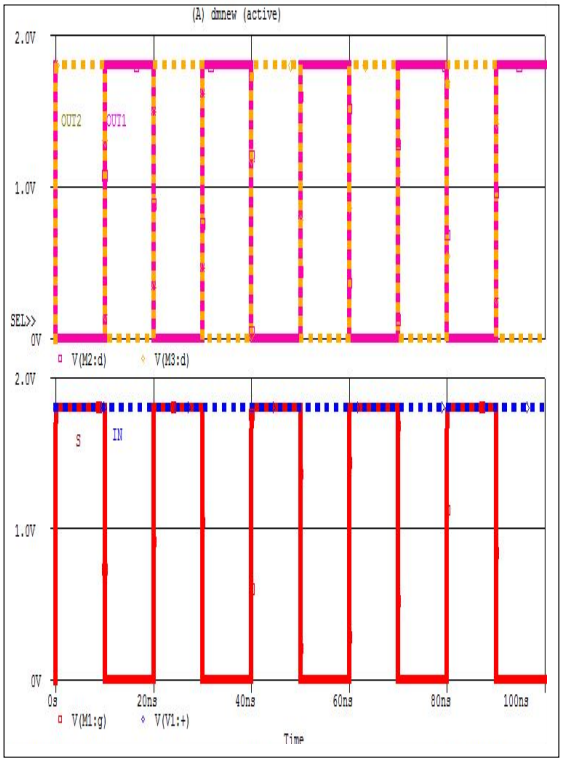
This research paper is arranged in seven sections including the current introductory Section I. Section II describes the CMOS logic implementation of 1:2 de-multiplexer, whereas, Section III, presents the pass transistor logic architecture implementation. Thereafter, Section IV deals with output current level of both architectures. Additionally, Section V and VI analyze the electrical characteristics to control the supply voltage, reduce the power dissipation and chip area. Finally, Section VII summarizes the important outcomes of the proposed work. Last section contains concluding remarks.

TABLE I. CHARACTERISTIC TABLE FOR 1:2 DE-MULTIPLEXERS.

Select Line (S)	Input (IN)	Outputs	
		Out1	Out2
0	0	0	0
0	1	1	0
1	0	0	0
1	1	0	1



(a)



(b)

Fig.1. Simulated gate level structure and Characteristic for 1:2 demultiplexer (a) gate level structure and (b) Input and output voltage results.

II. CMOS LOGIC IMPLEMENTATION

CMOS logic architecture is one of the most commonly used logic configuration employed in digital circuit designing but it has its own merits and demerits. Few are described here such as large numbers of transistors are required even to implement simple circuits like basic logic gates and inverter circuit. Fig. 2 depicts CMOS architecture of 1:2 de-multiplexers [2]. It is clear from the diagram that 14 transistors are required to implement this device. Six transistors for each AND gate and two for NOT gate, where S is selection line. The IN is input that is applied to both the AND gates. OUT1 and OUT2 represent output lines. The selection of these lines is dependent on terminal S. It can also be understood from the figure that large number of interconnects are used in this approach to connect numerous transistors. Therefore, CMOS logic is easy to design but very resource consuming [3].

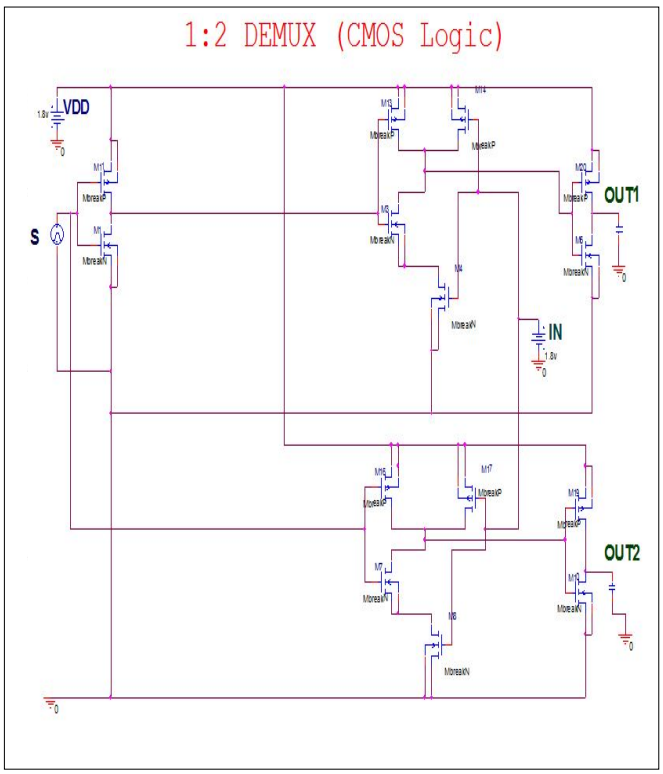


Fig.2. Schematic diagram of CMOS logic configuration of 1:2-demultiplexer.

III. PASS TRANSISTOR LOGIC ARCHITECTURE

The implementation of 1:2 de-multiplexer using pass transistor logic configurations is required only six transistors to implement the complete logic architecture. This means that number of transistors used in pass transistor architecture is less than 50% (Half) of the transistors utilized in CMOS architecture. Therefore, it is evident from the facts stated. Figure 3, show that the area consumption is 50% less using pass transistor logic architecture. Moreover, lesser interconnect lengths and fewer transistors allows a decrement in fabrication cost too. Moreover, the fabrication steps and resources are also decreased/ consumed less in pass transistor logic implementation. Therefore, results observed in both the architecture is stated that pass transistor architecture is more area efficient than ordinary CMOS architecture [2-5].

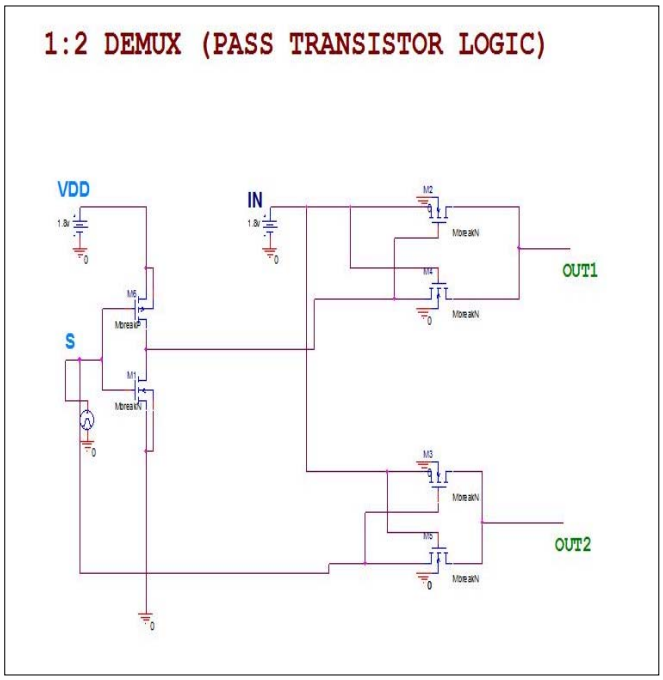


Fig. 3. Schematic diagram of pass transistor logic configuration of 1:2 de-multiplexers.

IV. Output Current Level Comparison Of Both Configurations

The comparison between CMOS and pass transistor logic architectures are discussed in this section. Besides this, analysis also done to identified the better driving capability among both the architectures. Output current levels of CMOS and pass transistor logic architecture are shown in Fig. 4 and Fig. 5, respectively. These characteristic plots are of the output current level of CMOS logic and pass transistor logic circuits that determine their driving capability. Results indicated that pass transistor logic configuration is the better options used in high speed and compact digital circuitry because of better driving capability, lower power dissipation and consumed low chip area. This can also noticed from Fig. 4, that maximum output current of de-multiplexer through CMOS logic reaches a value of 35µA approximately when a 'logic 1' value passes through it.

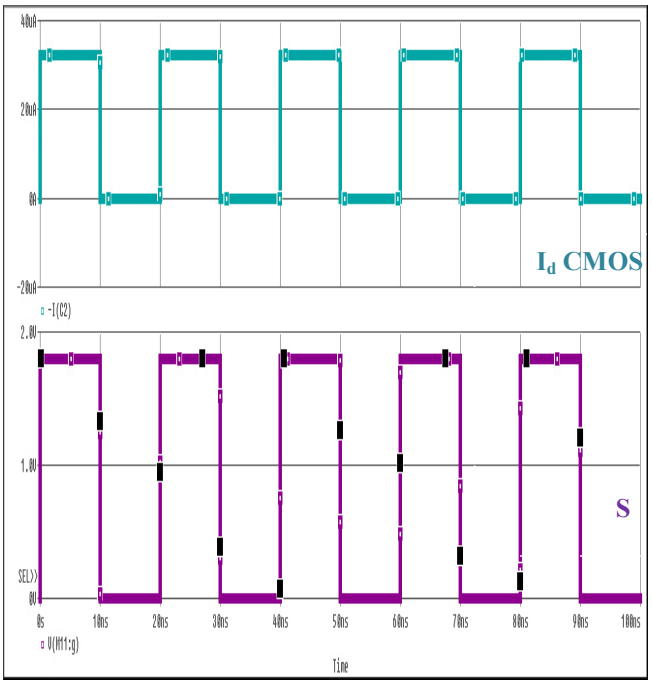


Fig. 4. Output current level for CMOS architecture of 1:2 de-multiplexer

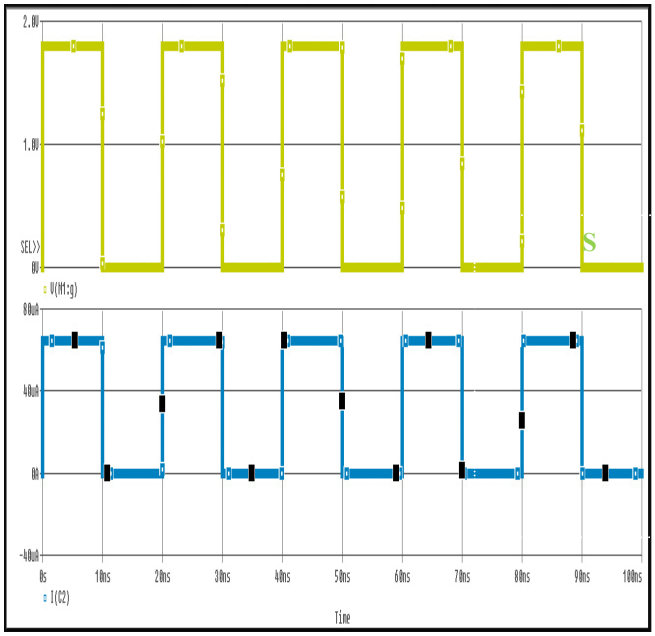


Fig. 5. Output current level for pass transistor architecture of 1:2 de-multiplexer 1.8V VDD

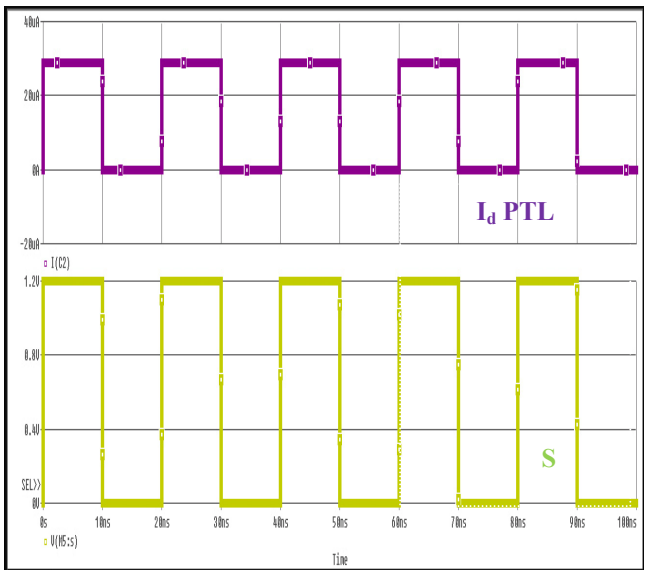


Fig. 6. Output current level for pass transistor architecture of 1:2 de-multiplexer 1.2V VDD

Now comparing the characteristics of the output current level of CMOS architecture with architecture shown in Fig. 2 and results observed large different in it. Figure 4, indicates this deficit. It can observed form the figure that out current level of de-multiplexer implemented through pass transistor architecture reaches a maximum value of 72µA that is more than the double of CMOS architecture. Therefore, we can say that 1:2 de-mux implemented through pass transistor logic has better driving capability over its counterpart implemented with CMOS logic architecture.

V. Reduction in Supply Voltage

Normally in all the cases average power dissipation of CMOS and MOS logic implementations is directly dependent on the supply voltage. This statement can be verified by Eq. (2).

$$P_{avg} = C_{load} \cdot V_{DD}^2 \cdot f_{clk} \qquad (1)$$

It is clear from Eq. (1) that supply voltage, V_{DD} is directly proportional to the average power dissipation, P_{avg} of the transistor. Any change in supply voltage is directly reflected on to the power dissipation. It is observed and discussed in Section IV that for the constant supply voltage pass transistor logic architecture is providing double current than CMOS logic architecture. Therefore pass transistor logic architecture reduce its supply voltage to an extent, when output current levels of both the architectures are same. This condition will further enable us to compare their power dissipation for similar output current. By Ohm's law, if reducing the supply voltage from 1.8V to 1.2V for pass transistor logic architecture. It get the maximum output current level of the architecture around 35µA. that is almost similar to the maximum output current level of CMOS architecture. Now power dissipation can be compared of the architectures as both are having similar output current level.

VI. Analysis of Power Dissipation and Performance Comparison for CMOS and Pass Transistor Logic

The power dissipation can be compared of the architectures as both are having similar output current levels. Power dissipation is the most important characteristic of any device in the era of portable devices, where most of the systems are working on a battery that has limited supply/backup time. Moreover, battery technology is not been able to cope-up with the transistor technology changes in recent times due to which a rift has been generated between power consumed by the device and power available to use. This gap can be fulfilling by the low power VLSI design methodologies that can reduce/control the power dissipation of the devices [5-7]. CMOS is power efficient logic but by observing Eq. (2), it can deduce that 1:2 De-multiplexer design implementation using pass transistor logic can further reduce the power dissipation of the circuits.

$$P_{avg} = \left(\sum \alpha_{Ti} . C_i . V_i \right) . V_{DD} . f_{clk} \quad (2)$$

Where α_{Ti} is corresponding node transition factor, C_i is parasitic capacitance associated with each node, V_i is node voltage, V_{DD} is supply voltage and f_{clk} is clock frequency. It is prominent from the equation that number of operating nodes also contribute to the overall power dissipation of the device. Since CMOS logic implementation requires larger number of transistors therefore operating points is higher in CMOS logic implementation than pass transistor logic implementation. Another important point *i.e.* supply voltage of pass transistor logic architecture. It is reduced by 33% (0.6V) making it further power efficient. Apart from Eq. (1) and (2) & Fig. 6 and 7 are also confirming our observation. Figure 6, indicate that maximum power dissipation of a transistor in CMOS logic architecture is increased to the level of 60µW that is also proved the Eq. (1) and (2). Moreover, it is the power dissipation of only one transistor. The overall power dissipation will be much more due to large number of transistor utilized in CMOS logic architecture implementation.

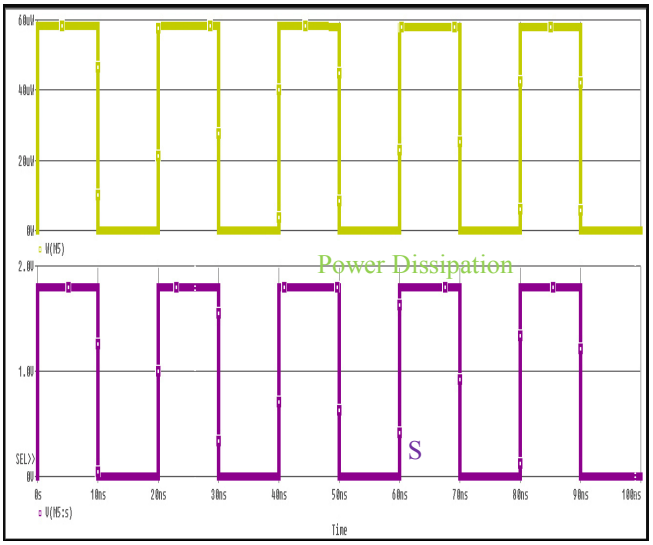


Fig. 7. Characteristic curve of power dissipation for CMOS architecture and pass transistor architecture of 1:2 de-multiplexer 1.8V VDD.

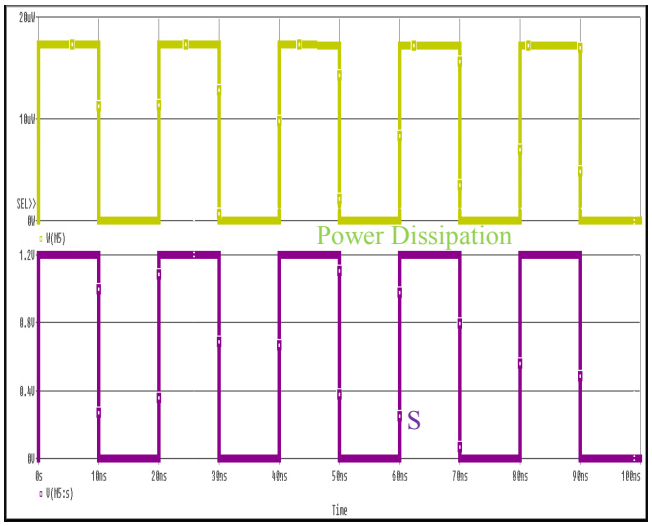


Fig. 8. Characteristic curve of power dissipation for pass transistor architecture of de-multiplexer 1:2 at 1.2V VDD.

On the other side, the pass transistor logic architecture characteristic wave form shown in Fig. 7, wherein, the power dissipation of individual transistors has an upper level only 18µW, that is 16 time less in comparison to the CMOS architecture. Moreover, the total number of transistors is 50% less (means half) in comparison to its counterpart (CMOS logic) that enhances the power efficiency. Besides this, 1:2 de-multiplexer architecture implementation using pass transistor logic configuration is more power efficient. Finally, to achieve an overall improved performance, the 1:2 de-multiplexer architecture is designed such that the pass transistor logic architecture are based on 6-transistors instead of often used conventional CMOS logic.

TABLE. II. COMPARISON OF PERFORMANCE PARAMETERS FOR CMOS AND PASS TRANSISTOR LOGIC CONFIGURATIONS

S. No.	Parameters	Pass Transistor Logic		CMOS Logic
		V_{DD}=1.8V	V_{DD}=1.2V	V_{DD}=1.8V
1.	Output current (I_D) (µA)	72	32	30
2.	Power Dissipation (µW)	60	18	60
3.	Chip Area	Less (6-T)	Less (6-T)	Larger(14-T)
4.	Interconnect Length	Small (6-T)	Small (6-T)	Large (14-T)

VII. CONCLUSION

This paper analyzed the performance of 1:2 De-Mux using PTLA and CLA. The results observed that approximately 50% of chip area is saved by using the pass transistor logic configuration as only six transistors (6-T) are employed to implement the 1:2 de-multiplexer while fourteen transistors (14-T) are used in CMOS logic architecture. The power supply is reduced by 33% observed due to processes with pass transistor logic. Moreover, 70% reduction in power dissipation is analyzed with pass transistor. Therefore, it can be concluded that the pass transistor logic implementation of 1:2 de-multiplexer gives better performance and consumes less chip area in comparison to CMOS logic architecture.

REFERENCES

[1] M. D. Ciletti and M. Morris Mano: Digital design, 4th Ed., Pearson, India, 2009.

[2] S. Byun, J. C. Lee, J. H. Shim, K. Kim and H. K. Yu, "A 10Gb/s CMOS CDR and DEMUX IC with a quarter-rate linear phase detector", IEEE Int. Solid-State Circuits Conf. (ISSCC 2006) Tech. Digest, pp. 1324-1333, San Francisco, CA, USA 6-9 Feb. 2006.

[3] S. M. Kang and Y. Leblebici: CMOS digital integrated circuits: Analysis and design", 3rd Ed, Tata McGraw-Hill, India, 2011.

[4] P. Buch, A. NaraOUT1n, A. R. Newton and A. Sangiovanni-Vincentelli, "Logic synthesis for large pass-transistor design", IEEE/ACM Int. Conf. Computer-Aided Design, (ICCAD-1997) Tech. Digest, pp. 663-670, San Jose, CA, USA, 09-13 Nov. 1997.

[5] R. Zimmermann and W. Fichtner, "Low power logic styles: CMOS versus pass-transistor logic", IEEE J. Solid-State Circuits, vol. 32, no. 7, pp. 1079 - 1090, Aug. 2002.

[6] S. R. Whitaker, "Combinational logic structures using pass transistors", United States Patent, Patent No. 4,541,067, 1985.

[7] D. A. Pucknell and K. Eshraghian, "Basic VLSI design", 3rd Ed, Prentice-Hall, India, 2006.