Reversible Logic Based Mapping of Quaternary Sequential Circuits Using QGFSOP Expression

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***Abstract*—Quaternary encoded binary circuits are more compact than their binary counterpart. Although several methods for designing binary reversible sequential circuits are presented, to the best of our knowledge, no design method for quaternary reversible sequential circuits has yet been reported in the literature. In this paper, we propose a design method for quaternary sequential circuits where the present state outputs are directly fedback to the next state determination circuit and that circuit is realized using QGFSOP expression as a cascade of one-digit, M-S, Feynman, and Toffoli gates. We also develop methods for making the sequential circuit falling-edge triggered and presettable using a quaternary Fredkin gate. As design examples, we present designs for up/down counters and universal registers. As there are no previous designs of quaternary sequential circuits, the closest comparison is made with designs of two-digit quaternary counter and universal register with designs of equivalent four-bit binary counter and universal register, respectively. In comparison to the equivalent binary designs, the proposed method requires less ancilla inputs with an increase in quantum cost.**

Keywords - Quaternary reversible sequential circuit, Toffoli gate realization, Fredkin gate realization, QGFSOP expression

I. INTRODUCTION

For a given binary function, a quaternary encoded realization requires half the number of primary input lines compared to a binary realization by encoding two bits into a quaternary digit. In quantum technology, interaction of more than two particles is nearly impossible to control. Therefore, the number of coupled quantum bits is a major limitation. Thus, in quantum technology, quaternary encoded realization of binary functions may be a favorable choice. Quaternary quantum circuits are realizable using ion-trap quantum technology [1]. The multiple-valued controlled gates proposed in [1] are commonly known as Muthukrishnan-Stroud (M-S) gates.

A number of customized designs of medium scale quaternary reversible combinational circuits are reported in [2-6]. A generalized method of designing arbitrary quaternary reversible combinational circuits using quaternary Galios field sum of products (QGFSOP) expression is reported in [7, 8]. All these designs are based on elementary quantum one-digit and M-S gates.

Though several design methods of binary reversible sequential circuits are reported in literature [9-13], as far as we know, no design method for quaternary reversible sequential circuits has yet been reported in the literature. In this paper, we propose a design method for quaternary reversible sequential circuits, where the present state outputs are directly fedback to the next state determination circuit and that circuit is realized using QGFSOP expression as a cascade of one-digit, M-S, Feynman, and Toffoli gates. We also develop methods for making the sequential circuit falling-edge triggered and presettable using a quaternary Fredkin gate. For this purpose, we propose a new realization method for multiple-input Toffoli gates using one-digit and M-S gates, which requires up to 95.22% less quantum costs (number of elementary quantum gates) than that in [14] for up to $n = 10$ inputs and requires only $(n - 3)$ zero-initialized ancilla inputs (working inputs other than the function inputs). For the first time in the literature, we propose realization of Fredkin gate using one-digit and M-S gates, which requires quantum cost of 18.

As design examples, we present designs for up/down counters and universal registers. As there are no previous designs of quaternary sequential circuits, the closest comparison is made with designs of two-digit quaternary counter and universal register with designs of equivalent four-bit binary counter and universal register in [13], respectively. The comparison shows that for both cases, quaternary designs require more quantum cost. Although the quaternary counter design requires slightly more ancilla inputs than the binary counter design, the quaternary register design requires nearly half the ancilla inputs than the binary register design.

The rest of the paper is organized as follows: In section II, we introduce the concept of QGFSOP expressions. We propose realizations for multiple-controlled Toffoli gates and Fredkin gate using one-digit and M-S gates in section III. In section IV, we discuss the reversible logic based mapping of quaternary sequential circuit using QGFSOP expression. Finally, we conclude the paper in section V.

II. BACKGROUND ON QGFSOP EXPRESSIONS

In the proposed mapping of quaternary sequential circuit, the next state is generated as a combinational function of the directly fedback present state output and the external input using QGFSOP expressions. Therefore, understanding of QGFSOP expression is very important. In this section, we briefly introduce the background of QGFSOP expression. Readers are referred to [7, 8] for more details.

The basis of a QGFSOP expression is the GF(4) arithmetic, which has a set of values $Q = \{0, 1, 2, 3\}$ and two binary operations: addition (denoted by $\oplus$) and

978-1-4799-8719-1/15 $31.00 © 2015 IEEE
DOI 10.1109/ISVLSI.2015.53

multiplication (denoted by · or juxtaposition). The GF(4) operations are shown in Table I. These operations are both commutative and associative. The multiplication operation is distributive over the addition operation.

TABLE I. GF(4) ADDITION (⊕) AND MULTIPLICATION (·) TABLES

⊕	0	1	2	3
0	0	1	2	3
1	1	0	3	2
2	2	3	0	1
3	3	2	1	0

·	0	1	2	3
0	0	0	0	0
1	0	1	2	3
2	0	2	3	1
3	0	3	1	2

There are 4! = 24 possible permutations of 0, 1, 2, and 3. Therefore, there are 24 possible permutative unitary transforms of a quaternary logic variable. These transforms are shown using truth tables in Table II. Each of the 24 transforms of Table II changes the value of a variable in reversible manner. Thus, we can define 24 reversible literals of a variable corresponding to 24 transforms. These literals are normally represented as x^z or $[z]x$, where x is the variable and $[z]$ is the transform. For example, x^{+1} or $[+1]x$ is the literal of the variable x corresponding to the transform [+1]. In this paper, when the context explicitly identifies the variable, we will represent a literal by its output vector. For example, the literal x^{+1} is represented by its output vector [1032].

TABLE II. QUATERNARY PERMUTATIVE UNITARY TRANSFORMS

Transform [z]	Input 0 1 2 3	Transform [z]	Input 0 1 2 3	Transform [z]	Input 0 1 2 3
[+0]	0 1 2 3	[13]	0 3 2 1	[123]	0 2 3 1
[+1]	1 0 3 2	[23]	0 1 3 2	[132]	0 3 1 2
[+2]	2 3 0 1	[012]	1 2 0 3	[0123]	1 2 3 0
[+3]	3 2 1 0	[013]	1 3 2 0	[0132]	1 3 0 2
[01]	1 0 2 3	[021]	2 0 1 3	[0213]	2 3 1 0
[02]	2 1 0 3	[023]	2 1 3 0	[0231]	2 0 3 1
[03]	3 1 2 0	[031]	3 0 2 1	[0312]	3 2 0 1
[12]	0 2 1 3	[032]	3 1 0 2	[0321]	3 0 1 2

A quaternary Galios field (QGF) product is defined to be a GF(4) product of two or more literals of one or more variables. For example, $x^{+3}x^{0213}y^{23}$ is a QGF product of three literals x^{+3}, x^{0213}, and y^{23} of two variables x and y. We define QGF product of two or three literals of the same variable as composite literals. For example, $x^{+1}x^{+2}x^{+3}$ is a composite literal. We also call the sum of the form (1 ⊕ composite-literal) as composite literal. For example, $(1 \oplus x^{+2}x^{23})$ is a composite literal. All the composite literals are irreversible in nature. We also represent a composite literal by its output vector. For example, the composite literal $x^{+1}x^{+2}x^{+3}$ is represented by its output vector [1000] and the composite literal $(1 \oplus x^{+2}x^{23})$ is represented by its output vector [1213]. A missing variable is represented as [- - - -]. We represent a QGF product using output vectors of the associated literals. For example, if $x^{+3}z^{23}$ is a QGF product of three variables x, y, and z, where the variable y is missing, then it is represented as [3210][- - - -][0132].

A QGFSOP expression is defined to be a GF(4) sum of two or more QGF products. For example, $F(x, y) = x^{+3}x^{0213}y^{23} \oplus xx^{+2}x^{+3}y^{+3}y^{0213} \oplus y^{13}$ is a QGFSOP expression. This QGFSOP expression is represented using output vectors of the associated literals as follows:

[1110][0132]
[0100][1110]
[- - - -][0321]

III. QUATERNARY REVERSIBLE GATES

In the proposed mapping technique of quaternary reversible sequential circuit, the QGFSOP expression representing the next state function will be realized as a cascade of one-digit, M-S, Feynman, and Toffoli gates. Moreover, the sequential circuit will be made falling-edge triggered and presettable using Fredkin gate. Therefore, understanding of these gates is very important. In this section, we will introduce these gates.

Each of the transforms of Table II can be realized as a one-digit gate [1]. The symbol of this gate is shown in Fig. 1(a), where z is any of the transforms. The quaternary M-S gate proposed in [1] is a controlled gate, whose symbol is shown in Fig. 1(b). The input x is the control input and appears at the output as $P = x$. The input y is the target input. When $x = 3$, the target output is $Q = [z]y$, otherwise $Q = y$. The one-digit and M-S gates are the elementary quantum gates and there quantum cost is assumed to be one.

The symbol of the quaternary Feynman gate is shown in Fig. 2(a). The input x is the control input and appears at the output as $P = x$. The input y is the target input. The target output $Q = x \oplus y$. The Feynman gate is a macro-level gate and is realized using one-digit and M-S gates. Realization of the Feynman gate is reproduced in Fig. 2(b) from [14], whose quantum cost is six.

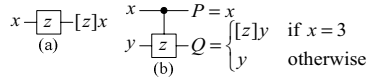

Figure 1. Symbol of (a) one-digit gate and (b) M-S gate.

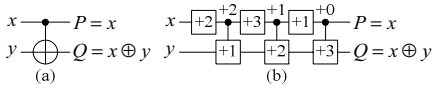

Figure 2. (a) Symbol and (b) realization of the Feynman gate.

For making the realizations of Toffoli and Fredkin gates modular, we introduce the concept of quaternary controlled Feynman gate, whose symbol is shown in Fig. 3(a). To avoid conflict with the symbol of Toffoli gate, the controlling point of the input x is represented by a ×. Outputs $P = x$ and $Q = y$. When $x \neq 3$ (that is, $xx^{+1}x^{+2} = 0$), then the target output $R = z$ making the gate an identity gate. When $x = 3$ (that is, $xx^{+1}x^{+2} = 1$), then the target output $R = y \oplus z$ making the gate Feynman gate controlled by the controlling input x. If the three one-digit gates of Fig. 2(b) are replaced by their corresponding M-S gates, then the realization will become controlled Feynman gate as shown in Fig. 3(b). If $x \neq 3$, then the three upper M-S gates are inactive and $Q = y$. In this case, if $y \neq 3$, then the three bottom M-S gates are inactive and $R = z$. If $y = 3$, then all three bottom M-S gates are active

and $R = 1 \oplus 2 \oplus 3 \oplus z = 0 \oplus z = z$. Thus, if $x \neq 3$, then $P = x$, $Q = y$, and $R = z$ making the gate an identity gate. If $x = 3$, then all the three upper M-S gates are active and the circuit becomes equivalent to that of Fig. 2(b) making it a controlled Feynman gate. The quantum cost of the controlled Feynman gate is six.

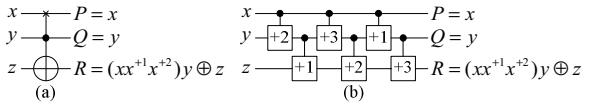

Figure 3. (a) Symbol and (b) realization of the controlled Feynman gate.

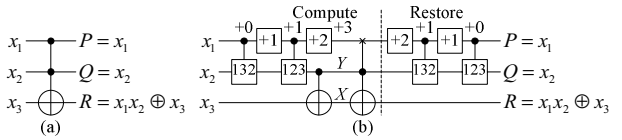

Figure 4. (a) Symbol and (b) realization of the three-input Toffoli gate.

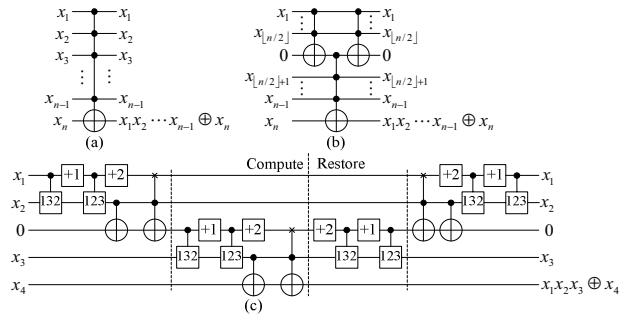

Figure 5. (a) Symbol and (b) architecture for realization of an n-input Toffoli gate. (c) Realization of a four-input Toffoli gate.

The symbol of quaternary three-input Toffoli gate is shown in Fig. 4(a). The inputs x_1 and x_2 are control inputs and appear at the output as $P = x_1$ and $Q = x_2$, respectively. The input x_3 is the target input. The target output $R = x_1x_2 \oplus x_3$. The Toffoli gate is a macro-level gate and is realized using one-digit and M-S gates. We propose a new realization of the three-input Toffoli gate in Fig. 4(b) that requires quantum cost of 20, which is less than that of [14]. When $x_1 = 0$, both the M-S gates of the compute part are inactive and $Y = x_2$, $X = Y \oplus x_3 = x_2 \oplus x_3$. The controlled Feynman gate is active and $R = Y \oplus X = x_2 \oplus x_2 \oplus x_3 = 0 \oplus x_3 = 0x_2 \oplus x_3 = x_1x_2 \oplus x_3$. When $x_1 = 1$, both the M-S gates of the compute part are inactive and $Y = x_2$, $X = Y \oplus x_3 = x_2 \oplus x_3$. The controlled Feynman gate is inactive and $R = X = x_2 \oplus x_3 = 1x_2 \oplus x_3 = x_1x_2 \oplus x_3$. When $x_1 = 2$, the second M-S gate of the compute part is active and $Y = [123]x_2 = 2x_2$, $X = Y \oplus x_3 = 2x_2 \oplus x_3$. The controlled Feynman gate is inactive and $R = X = 2x_2 \oplus x_3 = x_1x_2 \oplus x_3$. When $x_1 = 3$, the first M-S gate of the compute part is active and $Y = [132]x_2 = 3x_2$, $X = Y \oplus x_3 = 3x_2 \oplus x_3$. The controlled Feynman gate is inactive and $R = X = 3x_2 \oplus x_3 = x_1x_2 \oplus x_3$. Thus, for all values of x_1, the compute part computes $R = x_1x_2 \oplus x_3$. The restore part restores the values of x_1 and x_2 at the output. The last transform along x_1 is +0, so $P = [+0]x_1 = x_1$. When $x_1 = 0$ or $x_1 = 1$, then none of the M-S gates of the compute part and the restore part is active, so $Q = x_2$. When $x_1 = 2$, the second M-S gate of the compute part with transform [123] and the first M-S gate of the restore part with transform [132] are active. The transforms [123] and [132] are inverse of each other and $Q = [132][123]x_2 = [132]2x_2 = 3 \cdot 2x_2 = x_2$. When $x_1 = 3$, the first M-S gate of the compute part with transform [132] and the second M-S gate of the restore part with transform [123] are active and $Q = [123][132]x_2 = [123]3x_2 = 2 \cdot 3x_2 = x_2$. Thus, for all values of x_1, $Q = x_2$. Therefore, the circuit in Fig. 4(b) realizes a three-input Toffoli gate. The quantum cost of the compute part is 16 and that of the restore part is 4 making a total of quantum cost as 20.

A Toffoli gate may have more than three inputs. The symbol of an n-input ($n > 3$) Toffoli gate is shown in Fig. 5(a). Realization of the n-input Toffoli gate using two ($\lfloor n/2 \rfloor + 1$)-input Toffoli gates, one ($\lceil n/2 \rceil + 1$)-input Toffoli gate, and one zero-initialized ancilla input is shown in Fig. 5(b). The first ($\lfloor n/2 \rfloor + 1$)-input Toffoli gate produces $x_1x_2 \ldots x_{\lfloor n/2 \rfloor}$ along the ancilla input. The second ($\lfloor n/2 \rfloor + 1$)-input Toffoli gate restores the ancilla input. The ($\lceil n/2 \rceil + 1$)-input Toffoli gate produces $x_1x_2 \ldots x_{n-1} \oplus x_n$ at the target output. The first ($\lfloor n/2 \rfloor + 1$)-input Toffoli gate is realized using the compute part of the Toffoli gate and the second ($\lfloor n/2 \rfloor + 1$)-input Toffoli gate is realized using the compute part of the Toffoli gate by reversing the gate sequence and replacing each gate by its inverse gate, so that the inputs are restored at the outputs. The one-digit gates with transforms [+1], [+2], and [+3] are self-inverse gates. The Feynman and the controlled Feynman gates are also self-inverse gates. The M-S gates with transforms [123] and [132] are inverse of each other. The ($\lceil n/2 \rceil + 1$)-input Toffoli gate is realized using both compute and restore parts of the Toffoli gate. The quantum cost of an n-input Toffoli gate is $16(2n - 5) + 4$ and it requires $n - 3$ ancilla inputs. As an example of realizing an n-input Toffoli gate using the method of Fig. 5(b), the realization of a four-input Toffoli gate is shown in Fig. 5(c). The quantum cost and the number of ancilla inputs for up to $n = 10$ are computed and tabulated in Table III. The quantum cost is compared with that in [14]. We find that the present realization technique reduces the quantum cost in the range of 21.21% to 95.22% with the use of only $n - 3$ ancilla inputs.

The symbol of the quaternary Fredkin gate is shown in Fig. 6(a). The input x is the control input. The inputs y and z are the target inputs. The outputs are $P = x$, $Q = x^{+3}x^{0213}y \oplus xx^{+1}x^{+2}z$, and $R = xx^{+1}x^{+2}y \oplus x^{+3}x^{0213}z$. If the control input $x \neq 3$, then $xx^{+1}x^{+2} = 0$ and $x^{+3}x^{0213} = 1$. In this case the target outputs are $Q = 1y \oplus 0z = y$ and $R = 0y \oplus 1z = z$. Thus the target inputs y and z are passed directly to their outputs. If $x = 3$, then $xx^{+1}x^{+2} = 1$ and $x^{+3}x^{0213} = 0$. In this case the target outputs are $Q = 0y \oplus 1z = z$ and $R = 1y \oplus 0z = y$. Thus the target inputs y and z are swapped at the outputs. Realization of the Fredkin gate is shown in Fig. 6(b). If $x \neq 3$, then all three controlled Feynman gates will act as identity gates and the outputs will be $P = x$, $Q = y$, and $R = z$. If $x = 3$, then all three controlled Feynman gates will be active and the outputs

will be $P = x$, $Q = y \oplus (y \oplus z) = z$, and $R = z \oplus (y \oplus z) = y$. The quantum cost of this realization is 18.

TABLE III. QUANTUM COST (QC) AND NUMBER OF ANCILLA INPUTS (AI) FOR REALIZATION OF MULTIPLE-INPUT TOFFOLI GATES

n	QC [14]	QC (Present)	AI (Present)	% QC Improvement Over [14]
3	26	20	0	23.08
4	66	52	1	21.21
5	146	84	2	42.47
6	306	116	3	62.09
7	626	148	4	76.36
8	1266	180	5	85.78
9	2546	212	6	91.67
10	5106	244	7	95.22

If a composite literal has two or more a, where $a \in \{0, 1, 2, 3\}$, in the output vector, then the composite literal is realized along a a-initialized ancilla input using one-digit and M-S gates. For example, the realization of composite literal (+0,23) = [0111] = 1 ⊕ [1000] is shown in Fig. 7(a), which requires three quantum cost. Similarly, the realization of (1⊕+0,01) = [1123] = 1 ⊕ [0032] is shown in Fig. 7(b), which requires four quantum cost.

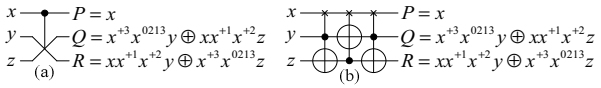

Figure 6. (a) Symbol and (b) realization of the Fredkin gate.

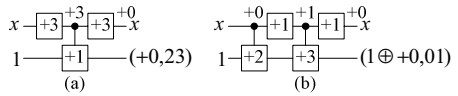

Figure 7. Realization of composite literals (a) (+0,23) and (b) (1⊕+0,01).

IV. REVERSIBLE MAPPING OF SEQUENTIAL CIRCUITS

Sequential circuit has memory called state of the circuit. The next state and the output of the sequential circuit are determined as combinational functions of the present state and the external input. The state is changed when the clock is applied to the circuit.

No method has yet been reported in the literature for designing quaternary reversible sequential circuits. Here we propose a special technique of designing quaternary reversible sequential circuits, where the present state is directly fedback to generate the next state. Let Q and Q^+ be the present state and the next state, respectively. Then Q^+ can be expressed as $Q^+ = Q \oplus Q \oplus Q^+ = Q \oplus Q^*$, where $Q^* = Q \oplus Q^+$ is the modified next state. Now, Q^* is determined as the combinational function of the present state and the external input. Let C be the clock. Then the next state is realized in the next state determination circuit as $Q^+ = Q \oplus CC^{+1}C^{+2}Q^*$. When $C \neq 3$ (i. e., $CC^{+1}C^{+2} = 0$), then $Q^+ = Q$, which provides the feedback of the present state through the next state determination circuit to maintain the present state. When $C = 3$ (i. e. $CC^{+1}C^{+2} = 1$), then $Q^+ = Q \oplus Q^*$, which generates the next state in the next state determination circuit. This generated next state is then passed to the present state output through a Fredkin gate when C goes from $C = 3$ to $C \neq 3$ (referred to as falling-edge), which then becomes the present state in the next clock. Thus, the circuit becomes a falling-edge triggered sequential circuit. The present state can also be asynchronously loaded using another Fredkin gate.

The proposed method of reversible mapping of sequential circuit is illustrated using a two-digit up/down counter. The state outputs are $Q1$ and $Q0$. The mode selector input M determines the direction of count. When $M \neq 3$, then it counts up. When $M = 3$, then it counts down. The output vector for the next state $Q0^+(M, Q1, Q0)$ is

[1230 1230 1230 1230 1230 1230 1230 1230 1230 1230 1230 1230 3012 3012 3012 3012]

Now, the output vector for the modified next state $Q0^*(M, Q1, Q0) = Q0(M, Q1, Q0) \oplus Q0^+(M, Q1, Q0)$ is

[1313 1313 1313 1313 1313 1313 1313 1313 1313 1313 1313 1313 3131 3131 3131 3131]

Now, the modified next state $Q0^*(M, Q1, Q0)$ is minimized as QGFSOP expression using the technique of [8], but the QGFSOP expression is represented using the notation adopted in this paper. The resulting minimized QGFSOP expressions is

$Q0^*(M, Q1, Q0) =$
[- - - -][- - - -][3131]
[2220][- - - -][- - - -]

Similarly, the resulting QGFSOP expression for the modified next state $Q1^*(M, Q1, Q0)$ is

$Q1^*(M, Q1, Q0) =$
[- - - -][3131][1000]
[1110][1010][3001]
[1110][0101][1003]

Now, the QGFSOP expressions for the next state equations are determined using the formula $Q^+ = Q \oplus CC^{+1}C^{+2}Q^*$. The minimized QGFSOP expressions for the next state equations of the two-digit up/down counter are

$Q0^+(C, M, Q1, Q0) =$
[- - - -][- - - -][- - - -][0123]
[0001][- - - -][- - - -][3131]
[0001][2220][- - - -][- - - -]

$Q1^+(C, M, Q1, Q0) =$
[- - - -][- - - -][0123][- - - -]
[0001][- - - -][3131][1000]
[0001][1110][1010][3001]
[0001][1110][0101][1003]

A reversible mapping of the two-digit up/down counter from the above QGFSOP expressions is shown in Fig. 8. Using the QGFSOP expressions of $Q1^+$ and $Q0^+$, we have

realized the "Next state determination" part in Fig. 8. In the "Feedback" part in Fig. 8, the two present states are copied using two Feynman gates and fedback to the "Next state determination" part of the circuit. In the "Load" part in Fig. 8, a mechanism has been provided for asynchronous parallel loading of the output states. When $L = 3$, the $D1$ and $D0$ data inputs will be loaded to the state output $Q1$ and $Q0$, respectively, through the Fredkin gates and they will become the present state. Then these newly loaded output states will be fed-back to the "Next state determination" part by the "Feedback" part of the circuit. As discussed latter, the "Next state determination" part determines the next state when the clock $C = 3$. Thus the output state loading should be made asynchronously only when $C \neq 3$ so that the loaded states are fed-back before the next state determination starts. When $L \neq 3$ then the Fredkin gates will pass the two state values provided by the "Edge trigger" part to maintain the output states unchanged. The QGFSOP expressions of next states $Q1^+$ and $Q0^+$ are realized in the "Next state determination" part in Fig. 8 as function of the fed-back present states $Q1$and $Q0$, the mode selector input M, and the clock C. As discussed earlier, when $C \neq 3$ (i. e., $CC^{+1}C^{+2} = 0$), then $Q^+ = Q \oplus CC^{+1}C^{+2}Q^* = Q$. In this case, the two outputs of the "Next state determination" part will simply be equal to the two fed-back present state values. When $C = 3$ (i. e. $CC^{+1}C^{+2} = 1$), then $Q^+ = Q \oplus CC^{+1}C^{+2}Q^* = Q \oplus Q^*$. In this case, the "Next state determination" part will determine the two next states. In the "Edge trigger" part of Fig. 8, a mechanism is provided for falling edge triggering of the circuit. When $C = 3$ then the Fredkin gate will provide the feedback to maintain the state output unchanged. At the same time, the "Next state determination" part will determine the next state. After that when the clock goes from $C = 3$ to $C \neq 3$ (falling-edge of the clock) then the Fredkin gates will pass the outputs of the "Next state determination" part to the state outputs through the "Load" part provided $L \neq 3$ is maintained. Thus, the sequential circuit becomes a falling-edge triggered circuit. The quantum cost of the circuit in Fig. 8 is 379.

A post-synthesis reduction of quantum cost is possible. As shown in the dashed box in Fig. 8, the top two control lines of two five-input Toffoli gates are the same. If these two Toffoli gates are decomposed, then we see from Fig. 5(c) that the last six gates of the restore part of the first Toffoli gate are in the reverse order of the first six gates of the compute part of the second Toffoli gate with each gate replaced by its inverse gate. So, these 12 gates will produce an identity effect and they can be eliminated. The quantum cost of these 12 gates is 32. Thus, the final quantum cost of Fig. 8 is 379 - 32 = 347. The circuit in Fig. 8 needs 14 ancilla inputs. In addition, the five-input Toffoli gate will require two more ancilla inputs. Thus, the total ancilla inputs are 14 + 2 = 16.

We have mapped a two-digit universal register as shown in Fig. 9. The state outputs are $Q1$ and $Q0$. The "Load" part of the circuit provides asynchronous load facility for parallel input. When $L = 3$ then the parallel input data $D1$ and $D0$ are loaded to the state outputs $Q1$ and $Q0$, respectively. Parallel outputs are taken from state outputs $Q1$ and $Q0$. The mode selector input M determines the direction of shift. When $M \neq 3$ then the circuit shifts the data right. In this case, the serial input is D_R and the serial output is $Q0$. When $M = 3$ then the circuit shifts the data left. In this case, the serial input is D_L and the serial output is $Q1$. Thus, the circuit is a two-digit universal register. The QGFSOP expressions for the next state equations are

$$Q0^+(C, M, D_R, D_L, Q1, Q0)=$$
[- - - -][- - - -][- - - -][- - - -][- - - -][0123]
[0001][- - - -][- - - -][- - - -][- - - -][0123]
[0001][0001][- - - -][0123][- - - -][- - - -]
[0001][1110][- - - -][- - - -][0123][- - - -]

$$Q1^+(C, M, D_R, D_L, Q1, Q0)=$$
[- - - -][- - - -][- - - -][- - - -][0123][- - - -]
[0001][- - - -][- - - -][- - - -][0123][- - - -]
[0001][0001][- - - -][- - - -][- - - -][0123]
[0001][1110][0123][- - - -][- - - -][- - - -]

Based on the above next state equations, a reversible mapping of a two-digit universal register is shown in Fig. 9. The quantum cost of the circuit in Fig. 9 is 359. After post-synthesis cost reduction the quantum cost becomes 295. The circuit has nine ancilla inputs. The four-input Toffoli gate realization requires one ancilla input. Thus, the total ancilla inputs are 9 + 1 = 10.

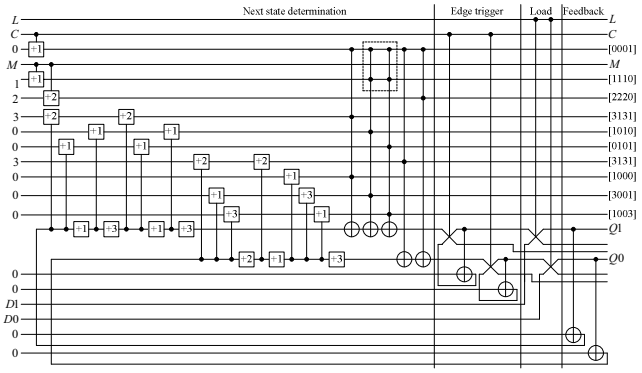

Figure 8. Reversible realization of a two-digit up/down counter with falling-edge triggering and parallel load.

The quantum costs and ancilla inputs for up/down counters and universal registers are calculated and summarized in Table IV. The designs of two-digit up/down counter and universal register are compared with their equivalent four-bit up/down counter and universal register from [13] in Table V. The quaternary designs require up to four-fold larger quantum cost than equivalent binary designs. However, quaternary universal register design requires almost half the ancilla inputs than equivalent binary design.

V. CONCLUSION

A quaternary encoded binary logic circuit requires 50% fewer primary inputs than its binary counterpart. Quaternary reversible circuits are realizable using ion-trap quantum

technology [1]. Therefore, efficient design methods of quaternary circuits are of great interest to researchers.

Though several designs of customized reversible quaternary combinational circuits [2-6] and a general technique of synthesizing reversible arbitrary quaternary combinational circuits [7, 8] are reported in the literature, to the best of our knowledge, no general design method of reversible quaternary sequential circuits has been reported yet. For the first time, we have proposed a QGFSOP-based design technique for a quaternary reversible falling-edge triggered sequential circuit. The QGFSOP expressions are minimized using the method of [8]. The QGFSOP expressions are realized as a cascade of one-digit, M-S, Feynman, and Toffoli gates. For this purpose, we have proposed a new realization technique of multiple-input Toffoli gates using one-digit and M-S gates. The proposed Toffoli gate realizations are by far the best and requires up to 95.22% less quantum costs than that in [14] for up to $n = 10$ inputs and requires only $(n - 3)$ zero-initialized ancilla inputs. A post-synthesis technique is used to reduce the quantum costs of the circuits by decomposing Feynman and Toffoli gates into one-digit and M-S gates. The design method also requires use of quaternary Fredkin gate. For this purpose, for the first time in the literature, we have proposed realizations of Fredkin gates using one-digit and M-S gates.

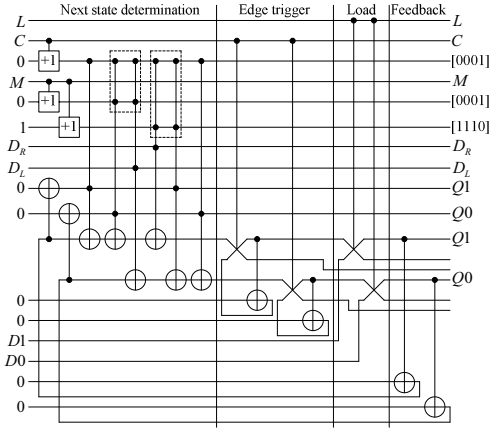

Figure 9. Reversible realization of two-digit universal register with falling-edge triggering.

TABLE IV. EXPERIMENTAL RESULTS OF REVERSIBLE SEQUENTIAL CIRCUIT DESIGN

Circuit	Initial Cost	Final Cost	Ancilla
Two-digit up/down counter	379	347	16
Three-digit up/down counter	752	751	24
Four-digit up/down counter	1217	1216	30
Two-digit universal register	359	295	10
Three-digit universal register	537	535	13
Four-digit universal register	715	711	16

The quantum costs and ancilla inputs of several sequential circuits are reported. In comparison to the equivalent binary designs in [13], this method requires more quantum costs but less ancilla inputs. Therefore, the proposed reversible mapping technique of quaternary sequential circuits is suitable for the quantum technology where the number of quantum digits is a major limitation.

TABLE V. COMPARISON OF QUATERNARY SEQUENTIAL CIRCUIT DESIGNS WITH EQUIVALENT BINARY DESIGNS IN [13]

Quaternary Designs			Binary Designs in [13]		
Circuit	Cost	Ancilla	Circuit	Cost	Ancilla
Two-digit up/down counter	347	16	Four-bit up/down counter	85	14
Two-digit universal register	295	10	Four-bit universal register	112	17

REFERENCES

[1] A. Muthukrishnan and C. R. Stroud Jr., "Multivalued logic gates for quantum computation," *Phy. Rev. A*, vol. 62, no. 5, pp. 052309/1-8, 2000.

[2] M. H. A. Khan, "Reversible realization of quaternary decoder, multiplexer, and demultiplexer circuits", *Engineering Letters*, vol. 15, no. 2, pp. 203-207, 2007.

[3] M. H. A. Khan, "A recursive method for synthesizing quantum/reversible quaternary parallel adder/subtractor with look-ahead carry", *J. Systems Architecture*, vol. 54, no. 12, pp. 1113-1121, Dec. 2008.

[4] M. H. A. Khan, "Synthesis of quaternary reversible/quantum comparators", *J. Systems Architecture*, vol. 54, no. 10, pp. 977-982, Oct. 2008.

[5] M. M. Khan, A. K. Biswas, S. Chowdhury, M. Tanzid, K. M. Mohsin, M. Hasan, and A. I. Kahn, "Quantum realization of some quaternary circuits," Proc. *2008 IEEE Region 10 Conference*, 2008, pp. 1-5.

[6] S. B. Mandal, A. Chakrabarti, and S. Sur-Kolay, "A synthesis method for quaternary quantum logic circuits," Proc. *Progress in VLSI Design and Test*, LNCS 7373, 2012, pp. 270-280.

[7] M. H. A. Khan and M. A. Perkowski, "GF(4) based synthesis of quaternary reversible/quantum logic circuits", *J. Multiple-Valued Logic Soft Computing*, vol. 13, pp. 583-603, 2007.

[8] M. H. A. Khan, N. K. Siddika, and M. A. Perkowski, "Minimization of quaternary Galois field sum of products expression for multi-output quaternary logic function using quaternary Galois field decision diagram", Proc. *IEEE Intl. Symp. Multiple-Valued Logic*, 2008, pp. 125-130.

[9] M.-L. Chuang and C.-Y. Wang, "Synthesis of reversible sequential elements," *ACM J. Emerging Tech.*, vol. 3, no. 4, pp. 1-19, 2008.

[10] H. Thapliyal and N. Ranganathan, "Design of reversible sequential circuits optimizing quantum cost, delay and garbage outputs," *ACM J. Emerg. Technol. Comput. Syst.*, vol. 6, no. 4, pp. 14:1–14:35, Dec. 2010.

[11] H. Thapliyal and N. Ranganathan, "Reversible logic-based concurrently testable latches for molecular QCA," *IEEE Trans. Nanotechnol.*, vol. 9, no. 1, pp. 62–69, Jan. 2010.

[12] H. Thapliyal, N. Ranganathan, and S. Kotiyal, "Design of testable reversible sequential circuits," *IEEE Trans. VLSI*, vol. 21, no. 7, pp. 1201 - 1209, June 2013.

[13] M. H. A. Khan, "Design of reversible synchronous sequential circuits using pseudo Reed-Muller expressions," IEEE Trans. VLSI, vol. 22, no. 11, pp. 2278-2286, 2014.

[14] M. H. A. Khan, "Quantum realization of multiple-valued Feynman and Toffoli gates without ancilla input," Proc. *IEEE Intl. Symp. Multiple-Valued Logic*, 2009, pp. 103-108.