A 32 BIT MAC Unit Design Using Vedic Multiplier and Reversible Logic Gate

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***Abstract*— The Vedic Multiplier and the Reversible Logic Gates has Designed and implemented in the multiply and Accumulate Unit (MAC) and that is shown in this paper. A Vedic multiplier is designed by using Urdhava Triyagbhayam sutra and the adder design is done by using reversible logic gate. Reversible logics are also the fundamental requirement for the emerging field of Quantum computing. The Vedic multiplier is used for the multiplication unit so as to reduce partial products and to get high performance and lesser area .The reversible logic is used to get less power. The MAC is designed in Verilog HDL and the simulation is done in Modelsim, Xilinx 14.2 and synthesis is done in both RTL compiler using cadence as well as Xilinx. The chip design for the proposed MAC is also carried out.**

Keywords—Reversible Logic, Urdhava Triyagbhayam, Quantum Computing, Kogge Stone Adder

I. INTRODUCTION

In the accumulate adder the previous MAC output and the present output will added and it consists of Multiplier unit, one adder unit and both will get be combined by an accumulate unit. The major applications of Multiply-Accumulate (MAC) unit are microprocessors, logic units and digital signal processors, since it determines the speed of the overall system [13]. The efficient designs by MAC unit are Nonlinear Computation like Discrete Cosine or wavelet Transform (DCT), FFT/IFFT. Since, they are basically executed by insistent application of multiplication and addition, the entire speed and performance can be compute by the speed of the addition and multiplication taking place in the system. Generally the delay, mainly critical delay, happens due to the long multiplication process and the propagation delay is observed because of parallel adders in the addition stage.

The main idea of this paper is comparison of area, speed and other parameters of Conventional MAC unit with the Vedic MAC design.

II. LITERATURE SURVEY

A. MAC Unit

A multiplying function can be carried out in three ways: partial product Generation (PPG), partial product addition (PPA), and final conventional addition. The two bottle necks that should be considered are increasing the speed of MAC are partial product reduction and accumulator block.

The 32 bit Mac design by using Vedic multiplier and reversible logic gate can be done in two parts. First, multiplier unit, where a conventional multiplier is replaced by Vedic multiplier using Urdhava Triyagbhayam sutra.

Multiplication is the fundamental operation of MAC unit [1]. Power consumption, dissipation, area, speed and latency are the major issues in the multiplier unit. So, to avoid them, we go for fast multipliers in various applications of DSP, networking, etc. There are two major criterion that improve the speed of the MAC units are reducing the partial products and because of that accumulator burden is getting reduced. The basic operational blocks in digital system in which the multiplier determines the critical path and the delay. The (log2N + 1) partial products are produced by 2N-1 cross products of different widths for N*N. The partial products are generated by Urdhava sutra is by Criss Cross Method. The maximum number of bits in partial products will lead to Critical path.

The second part of MAC is Reversible logic gate. In modern VLSI, fast switching of signals leads to more power

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dissipation. Loss of every bit of information in the computations that are not reversible is kT*log2 joules of heat energy is generated, where k is Boltzmann's constant and T the absolute temperature at which computation is performed. In recent years, reversible logic functions has emerged and played a vital role in several fields such as Optical, Nano, Cryptography, etc.

III. DESIGN OF MAC ARCHITECTURE

The design of MAC architecture consists of 3 sub designs.

- Design of 32×32 bit Vedic multiplier.
- Design of adder using DKG gate reversible logic.
- Design of accumulator which integrates both multiplier and adder stages.

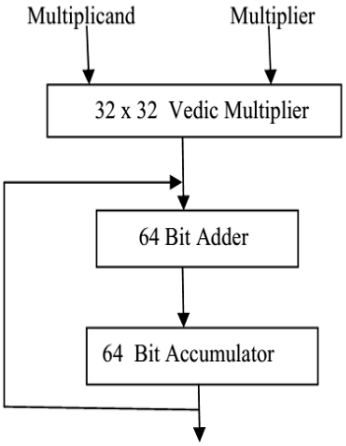


Fig 1:Modified MAC Architecture

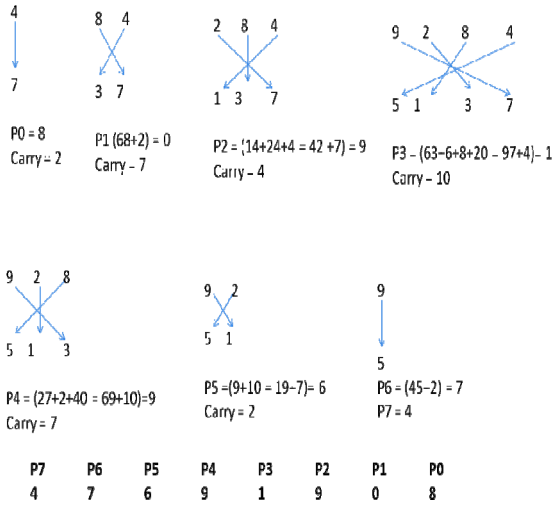
A. 32 x 32 bit Vedic Multiplier

Vedic mathematics is an ancient system of mathematics, which was formulated by Sri Jagadguru Swami Bharati Krishna Tirthaji (1884 - 1960). After a research of eight years, he developed sixteen mathematical formulae from Atharvana Veda[11]. The sutras (aphorisms) covered each and every topic of Mathematics such as Arithmetic, Algebra, Geometry, Trigonometry, differential, integral, etc., The word "Vedic" is derived from the word "Veda" which means the power house of all knowledge and divine [2, 3]. The proposed Vedic multiplier is based on the "Urdhava Triyagbhayam" sutra (algorithm). These Sutras have been traditionally used for the multiplication of two numbers in the decimal number system. In this work, we will utilize similar techniques to solve the binary number system to make the new aphorism, which will be more compatible for the digital systems. It is a general multiplication formula applicable to all cases of multiplication.

B. Urdhava Triyagbhayam Sutra

It literally means "Vertically and Crosswise". Shift operation is not necessary because the partial product calculation will perform it in a single step, which in turn saves time and power. This is the main advantage of the Vedic multiplier [14].

An example for the Urdhva Triyagbhayam sutra is as follows: 9284 * 5137



IV. IMPLEMENTATION OF VEDIC MULTIPLIER USING MODEL ARCHITECTURE IN DESIGN

The following fig. 2 shows the design of a 16×16 Vedic multiplier using an 8×8 Vedic multiplier and the design can be implemented using Verilog HDL. Using a 16×16 Vedic multiplier we can design 32 ×32 Vedic multiplier with carry save adder as shown in fig.3. We have modified the final adder stage with the Kogge stone adder which is more efficient than the Carry save adder which is shown in the fig .4.

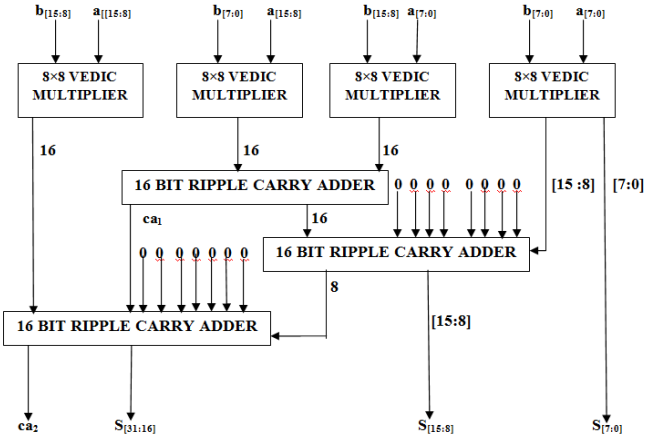


Fig 2: 16×16 Vedic multiplier using 8×8 Vedic multiplier

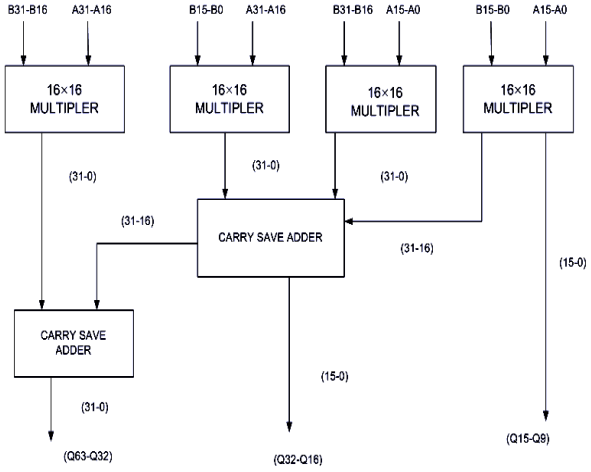


Fig 3: 32 × 32 Vedic Multiplier with Carry save Adder

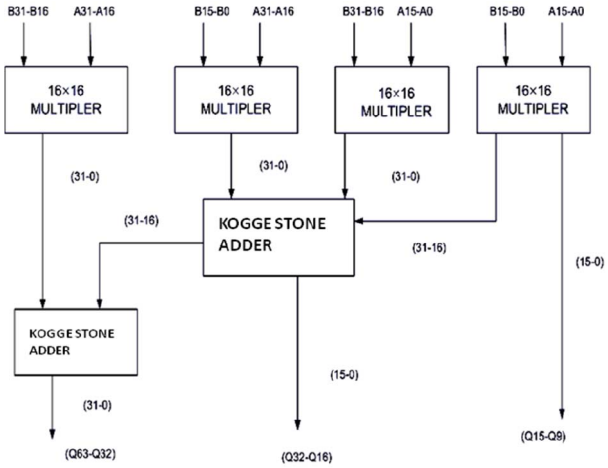


Fig 4: 32 × 32 Vedic Multiplier with Kogge Stone Adder

By using the Vedic multiplier we can achieve lesser partial products as the table shows that the multiplier and adder stages for Vedic multiplier for higher bit are lesser as compared to the conventional multiplier.

The multiplier design has been simulated and synthesized using Xilinx. The floor plan, device and port details of the multiplier are shown in the fig. 5.

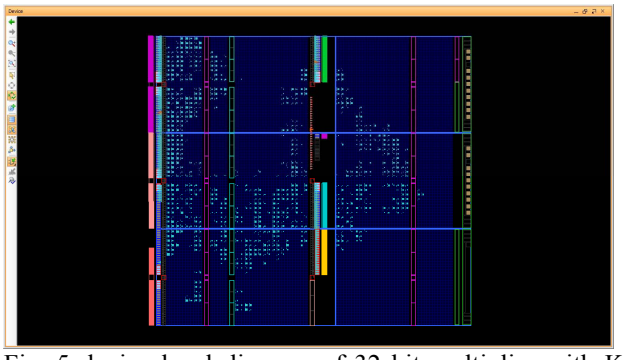


Fig. 5 device level diagram of 32 bit multiplier with Kogge Stone Adder

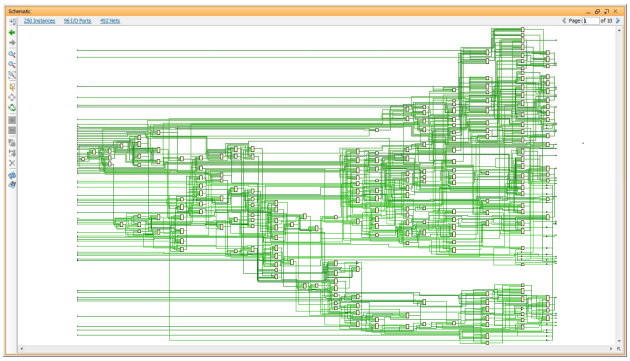


Fig . 5a. schematic floor plan of 32 bit Vedic multiplier with Kogge Stone Adder

V. KOGGE STONE ADDER

It's a parallel prefix adder, which is the one of the fastest adder. Carry stages: $\log_2 n$; The number of cells: $n(\log_2 n-1)+1$; Maximum fan-out: 2 (extra wiring). So, it will reduce the power consumption as well as the power dissipation.

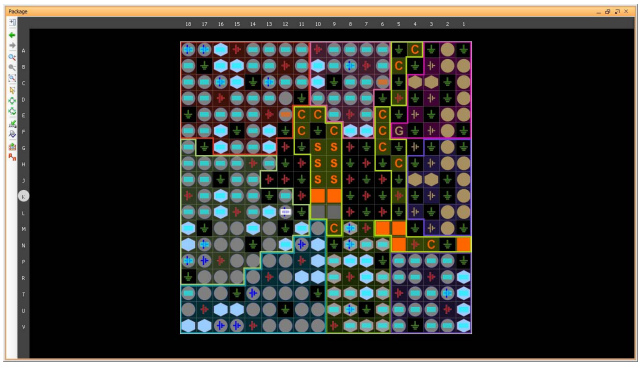


Fig. 5b. I/O package of 32 bit Vedic multiplier with Kogge Stone Adder

Table 1: comparison of no of additions and multiplications required in various Multipliers

M=MULTIPLIICATION A= ADDITION

Multiplier	8 x 8 BIT	16x16 BIT	32 x 32 BIT
Conventional	64M 56A	256M 240A	1024M 1022A
Vedic multiplier with RCA	8M 4A	16M 8A	32M 16A
Booth	40M 26A	96M 72A	288M 243A
Vedic multiplier with Kogge stone Adder	8M 4A	17M 7A	35M 13A

VI. DESIGN OF ADDER USING REVERSIBLE LOGIC DKG GATE

A. Reversible logic

Reversible logic is a unique technique (different from other logic). Loss of information is not possible in here. In this, the numbers of outputs are equal to the number of inputs.

1. General consideration for reversible logic gate

A Boolean function is reversible if each value in the input set can be mapped with a unique value in the output set. Landauer [18] proved that the usage of traditional irreversible circuits leads to power dissipation and Bennet [17] showed that a circuit consisting of only reversible gates does not dissipate power. In the design of reversible logic circuits, the following points must be kept in mind to achieve an optimized circuit:

- Fan-out is not permitted
- Loops or feedbacks are not permitted
- Garbage outputs must be Minimum
- Minimum delay
- Minimum quantum cost
- Zero energy dissipation [17]

2. DKG Gate

A 4* 4 reversible DKG gate [6] that can work singly as a reversible full adder and a reversible full subtractor is shown below. If input A=0, the DKG gate works as a reversible Full adder, and if input A=1 then it works as a reversible Full subtractor. It has been verified that a reversible full-adder circuit requires at least two or three garbage outputs to make the output combinations unique [5], [6].

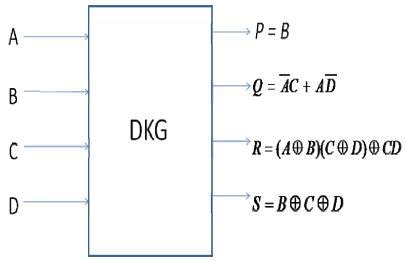


Fig. 6a [6] DKG gate

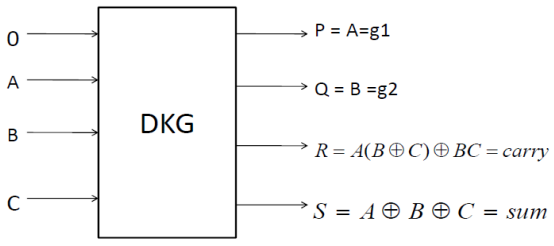


Fig. 6b DKG gate as a Full adder

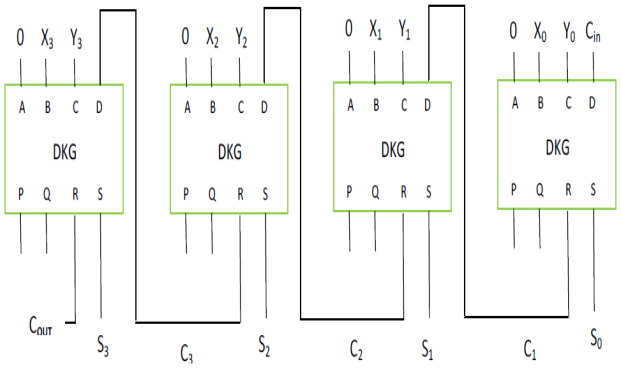


Fig. 6c Parallel adder using DKG gate

VII. ACCUMULATOR STAGE

Accumulator has an important role in the DSP applications in various ranges and is a very basic and common method. The register designed in the accumulator is used to add the multiplied numbers. Multiplier, adder and an accumulator are forming the essential foundation for the MAC unit. The conventional MAC unit has a multiplier and multiplicand to do the basic multiplication and some parallel adders to add the partial products generated in the previous step. To get the final multiplication output we add the partial product to these results. Vedic Multiplier has put forward to intensify the action of the MAC Unit. The suggested MAC is compared with the conventional MAC and the results are analyzed. The results obtained using our design had better performance when compared to the pervious MAC designs.

VIII. RESULT AND DISCUSSION

The modified multiplier using the Kogge Stone Adder is fast and the design of 32 bit MAC is done in Modelsim. The synthesis is performed out in Cadence RTL compiler. The above design is implemented in Verilog Code using mentor graphics modelsim 6.5b. Synthesis of the RTL code is done using Cadence RC compiler in 45nm technology. RTL Schematic view is given in the fig. 7. Comparison of area, speed and power reports is made with other methods as shown in table 2.

Table 2: Analysis report of 32-bit MAC using Booth, Wallace tree and Vedic with Reversible logic multiplier.

PARAMETER	Booth multiplier	Booth recoded Wallace tree multiplier	Vedic multiplier with Kogge Stone Adder and reversible logic (proposed model)	Vedic multiplier and reversible logic (proposed model)
POWER(nw)	18398.67	17567.678	15621.12	15546.567
SPEED(ns)	6.567	6.436	4.932	5.667
AREA(um^2)	2322	2379	1972	2123

Comparison of parameters with different 2 bit MAC architectures is shown in fig. 8

Simulation of 32 bit MAC output is shown in fig. 9

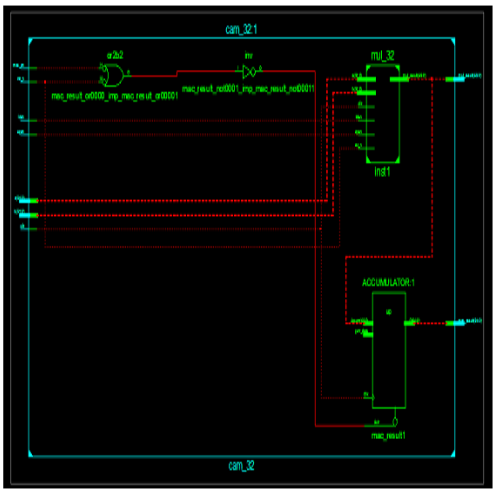


Fig 7: RTL schematic of 32 bit MAC architecture

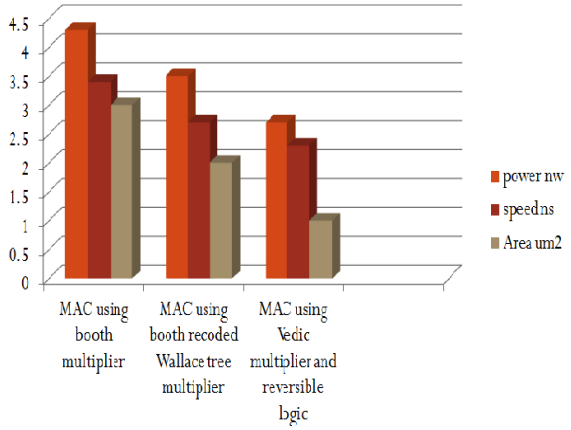


Fig 8: Comparison of different 32 BIT MAC Architectures

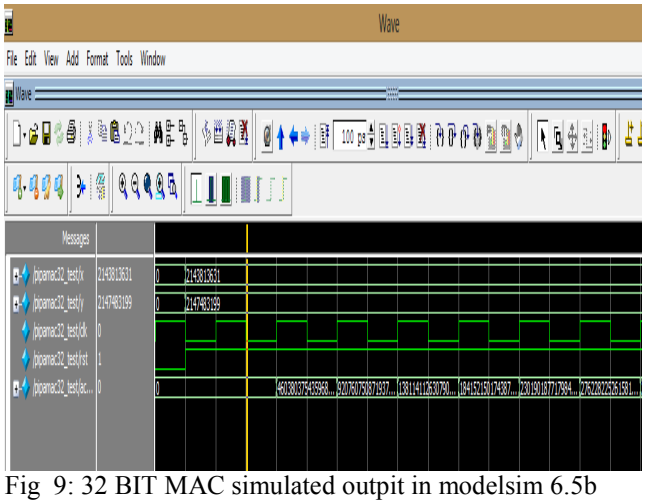


Fig 9: 32 BIT MAC simulated outpit in modelsim 6.5b

IX. Conclusion and Future Work

The results obtained by the design of Vedic multiplier with 32 bits and reversible logic are quite good. The work presented is based on 32 – bit MAC unit with Vedic Multipliers. We have designed MAC unit basic building blocks and its performance has been analyzed for all the blocks. Therefore, we can say that the Urdhava Triyagbhayam sutra with 32-bit Multiplier and reversible logic is the best in all aspects like speed, delay, area and complexity as compared to other architectures which are shown in table 2.

Many researchers are reconfiguring the structure of MAC unit, which is the basic block in different designs and aspects especially using reversible logic which evolves recent days. Spectrum Analysis and Correlation linear filtering which are the applications of transform algorithm further add to the field of communication, signal and image processing and instrumentation, and some other. Combining the Vedic and reversible logic will lead to new and efficient achievements in developing various fields of Mathematics, science as well engineering.

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