

# Towards reversible QCA computers: reversible gates and ALU

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**Abstract**—This work presents a novel implementation of reversible gates and reversible ALU, all based in quantum-dot cellular automata (QCA). QCA has been considered as an alternative for field-effect transistors due to its quite small size (nanometers), ultra-low power consumption and clock rate (terahertz range). On the other hand, reversible computation is a new paradigm where all logic operations can be performed in an invertible way. This feature is important to different technologies, such as quantum computing, adiabatic circuits, low power computation, etc. Regarding low power consumption, QCA has been seen as a promising technology for approaching the thermodynamic limit of computation and this work focus on designing a QCA reversible ALU in order to go beyond that limit, bridging the gap between QCA technology and reversible components. In a bottom-up approach, we first discuss QCA reversible gates and a few design choices. We also present the ALU's QCA design, demonstrate the functionality, test and validate the proposed architecture using QCA Designer simulator. Due to the importance of these new computational paradigms, this study is central in consolidating possible emerging technologies.

## I. INTRODUCTION

In the next few decades we will approach a turning point in the way we build computers. The CMOS transistor has its feature size approaching the range of a few nanometers, which makes the device's behavior deviate from the ideal switch. Despite there is no mature technology yet, many new devices are being studied as replacements for CMOS transistors, many of which do not even use electron charge as the state variable [1].

One of the research topics with the potential for the design of new hardware components is Quantum-dot Cellular Automata (QCA). QCA is a potential alternative to CMOS transistor-based circuits. It is a nanoscale technology where a cell has nano size, ultra-low power consumption and promising high clock rate (order of tera-Hertz) [2].

Furthermore, there is a fundamental problem, technology independent, underlining the conventional way we compute. In 1961, Rolf Landauer argued that any irreversible computational process, e.g., AND, OR, XOR, implies the lost of  $kT \ln(2)$  joules per bit erased, where  $k$  is the Boltzmann constant and  $T$  is the temperature [3]. The validity of this thermodynamic limit of computation, also known as Landauer's principle, has been questioned since its proposal. Only recently, in 2012, it was experimentally verified, proving the physical limit of irreversible computation [4].

Between Landauer's proposal and its experimental proofs, a few researchers came up with ways to avoid this limit. One possible solution is achieved by building the process using reversible primitives [5]. These primitives, also known as reversible gates, are information preserving, i.e., they have one-to-one relation (bijective functions) between inputs and outputs.

Although QCA has been seen as a promising technology for approaching the thermodynamic limit of computation [6], there is still the need to design new hardware components (gates and circuits) with this technology. In an effort to go beyond that limit, bridging the gap between QCA technology and reversible components, we focus on designing different QCA reversible gates and circuits.

The main contributions of our work are as follows. First, we implemented different reversible gates based in previous proposed abstract gates. Second, we have implemented a reversible Arithmetic and Logic Unit applying the proposed gates. Third, we demonstrate the functionality and validate the proposed system using QCA Designer simulator within the time-dependent coherence vector engine.

The remaining of this paper is organized as follow: In section 2 we present an introduction to QCA. The related works are analyzed and discussed in section 3. Following, the proposed reversible gates and ALU designs layout and simulation results are presented in section 4. The discussion about our design choices and implications are presented in section 5. Finally, section 6 concludes the paper and presents some relevant extensions of this work.

## II. QUANTUM-DOT CELLULAR AUTOMATA

QCA technology consists of a group of cells which, when combined and arranged in a particular way, are able to perform computational functions. QCA technology transfers information by means of the polarization state of various cells in contrast to traditional computers, which use the flow of electrical current to transfer information [2].

QCA cells are the basic units of QCA circuit and they are typically composed of four quantum dots located at the corners of a square. A dot, in this context, is just a region where an electric charge can be located or not. Each cell has two free and mobile electrons, which are able to tunnel between adjacent dots. Also, a back plane voltage controls the cell occupancy. Tunneling to the outside of the cell is not allowed due to a

high potential barrier. The Coulomb interaction between the electrons tends to locate them at opposing diagonals, as shown in Fig. 1 (a). An isolated cell may be in one of two equivalent energy states. These states are called cell polarizations  $P = +1$  and  $P = -1$ . So, it is possible to codify binary information by considering that  $P = +1$  represents the value 1 and that  $P = -1$  represents the value 0.

When two cells are placed near each other, the polarization of one cell will influence the polarization of the other cell. In this case, the two possible polarization states of the second cell will not be equivalent. For example, consider that a cell (cell 1) has its polarization fixed at  $P1 = +1$  and it is placed next to a second cell (cell 2). The distribution of charges of cell 2 is influenced by the distribution of charges in cell 1, which is then responsible for the polarization of cell 2 ( $P2$ ). So, cell 2 tends to have the same polarization as cell 1, reducing the Coulomb interaction between all the electrons involved. Following the same rule, a wire can be built by placing several QCA cells in a row, as shown in figure 1 (b).

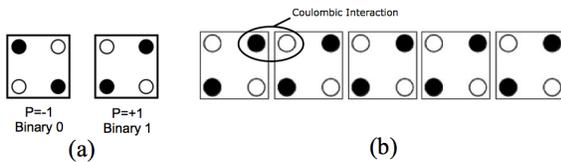


Fig. 1. (a) Possible polarizations of QCA cells with four quantum dots. Black dots represent the electrons positions and (b) A QCA wire.

QCA logic devices are designed by selecting the placement of QCA cells in a way that leverages the interaction between them. The two fundamental QCA gates, inverter and majority gates, are presented and explained in details. When cells are placed diagonally to each other, they tend to have reverse polarizations due to the repulsion between electrons. This feature can be explored to build an inverter, such as the one shown in Figure 2 (a).

The majority gate (Fig. 2 (b)) is the most important basic QCA logic device as it can be used to build AND and OR gates, besides being used to build more complex devices. The device cell at the center of the gate has its lowest energy when it assumes the polarization of the majority of the three input cells because this is the configuration where the repulsion between the electrons in the three inputs cells and the electrons in the device cell is the smallest. Observe in Fig. 2 (b) that, even though input cell A has the polarization that represents binary 0, the output cell has the same polarization as cells B and C, which are the majority in this case. Also, if input cell A is always fixed at binary 0, an AND gate with two inputs (B and C) is defined. In the same way, if the same cell A is always fixed at binary 1, an OR gate is formed. With ANDs, ORs, and inverters, any logic function can be implemented. So, any computational circuit can be fulfilled with QCA paradigm.

In order to build more complex QCA devices, one not only needs to select carefully the placement of QCA cells but also needs to synchronize the information, in order to avoid having a signal reaching a logic gate and propagating before the other inputs reach the gate. This characteristic is extremely important in QCA circuits, guaranteeing its correct operation. This feature is achieved by QCA clock. The clock is

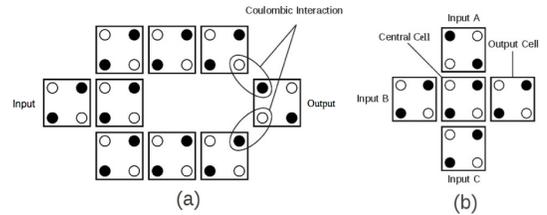


Fig. 2. (a) A QCA inverter and (b) A QCA Majority Gate.

an electrical field, which controls the tunneling barriers within a cell, thus keeping control when a cell might or might not be polarized. The clock can be applied to groups of cells (clock zones). In each zone, a single potential can modulate the barriers between the dots. The scheme of clock zones permits a cluster of QCA cells to make a certain calculation and then its states are frozen and its outputs can be used as inputs to the next clock zone.

### III. RELATED WORK

Currently, there are few works about QCA and reversible logic. In [7] the authors propose an alternative clock that requires a modification in the timing of the clocking signals so that bit information is simply held in place by the clock until a computational block is complete, then erased in the reverse order of computation. This approach is called "Bennett clocking" and results in ultralow power dissipation without additional circuit complexity. However, this new clocking scheme induces a delay in signal propagation, since all cells in a circuit must be totally polarized, and then completely depolarized in reverse. This disrupts the inherent pipeline of QCA circuits. In order to minimize this problem, an architecture for QCA circuits which combines the conventional clocking scheme and regions with "Bennet clocking" scheme were proposed [8]. This gathers together the low power of reversible circuits with the high throughput of the conventional QCA pipeline.

In a different approach, Thapliyal and Ranganathan proposed the design of testable sequential circuits based on QCA Fredkin gates [9]. In this case, the reversible Fredkin gate is designed based on QCA. The main goal in their work was the testability, more specifically the detection of single missing/additional cell defect faults. Sen [10] and collaborators extended Thapliyal work proposing a reversible ALU based in QCA multiplexers [10]. However, to the best of our knowledge, the aforementioned works lack realistic considerations about quantum-mechanical characteristics of the device. They only use the bistable simulation engine of QCADesigner software.

Despite the few studies relating QCA circuits being applied to reversible logic, QCA has been widely applied to the development of other logic circuits, as can be found in some recent studies [11] [12]. This demonstrates the importance of research on this technology for future computers. Beyond that, this work goes a step forward dealing with logic reversibility, which is fundamental for fault detection and energy efficiency.

### IV. REVERSIBLE GATES AND ALU QCA'S DESIGN

There are several reversible logic gates proposed since Toffoli and Fredkin's seminal work. Although we have designed

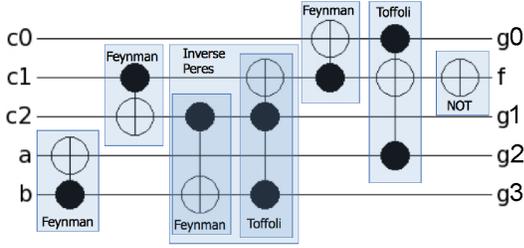


Fig. 3. Gupta's ALU.

TABLE I. ALU'S OPERATIONS.

c0	c1	c2	Function (f)
0	0	0	constant 1
0	0	1	a OR b
0	1	0	a NAND b
0	1	1	a XOR b
1	0	0	a NXOR b
1	0	1	a AND b
1	1	0	a NOR b
1	1	1	constant 0

twelve different gates using the QCA technologies, we present here only those applied in our reversible ALU implementation.

The first one implemented was the Toffoli gate. Its outputs  $P$  and  $Q$  are exactly the two first inputs, which work as control lines. This gate flips the third input if and only if each control input is high. Toffoli gate's equations are:  $P = A, Q = B, R = AB \oplus C$ . The Feynman gate, also known as Controlled NOT, implements the follow logic expression:  $P = A, Q = A \oplus B$ . Peres gate logic could be understood as a Half-adder circuit:  $Q = A \oplus B$  implements the sum,  $R = AB \oplus C$  implements the carry and  $P = A$  only exists to preserve the reversibility.

Applying the presented gates, we built, in a modular fashion, the QCA implementation of an ALU found in RevLib [13] and introduced in [14] (Figure 3). This ALU has 2 one-bit operators ("a" and "b") and three other input signs to select the function ("c0", "c1" and "c2"). The output "f" maps the desirable function and all other "g" outputs, which are different from each other, only exist to preserve reversibility. Table I presents ALU's operations.

Figure 4 shows our QCA realization of some reversible gates and the Gupta's ALU. Table II reports area, complexity and speed parameters of the individual gates and the ALU.

All designs, gates and ALU, were verified using the QCADesigner 2.0.3 with the coherence vector engine. We used the following simulation parameters: Cell Width = 18 nm, Cell Height = 18 nm, Dot Diameter = 5nm, Number of Samples = 12.800, Convergence Tolerance = 0.001, Radius of effect = 80 nm, Relative permittivity = 12.9, Clock high = 9.8E-22J, Clock low = 3.8E-23J, Clock amplitude factor = 2, Layer Separation = 11.5 nm, Maximum iterations per sample = 100.

Despite that the ALU has been tested with all possible input combination, Figure 5 only shows the simulation results

TABLE II. PERFORMANCE ANALYSIS.

Circuit	Area (cells)	Cells	Latency (cycles)
Toffoli Gate	27 x 26	155	3
Feynman Gate	20 x 21	102	2.25
ALU	142 x 66	1097	15

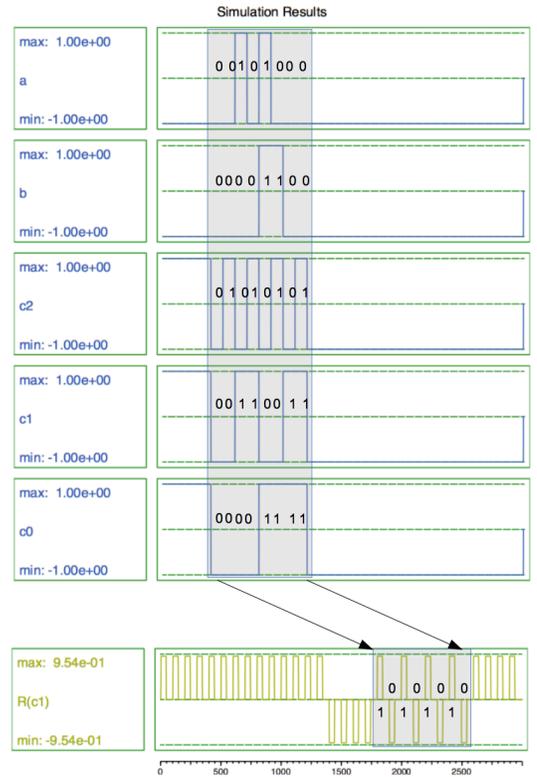


Fig. 5. Simulation results.

of a few cases for the sake of clarity (all functions presented in table I). We can see the expected result delayed by 15 clock cycles, which is the slowest path between input and output.

## V. DISCUSSION

It is important to report some of our design choices due to the implications in gates and systems performances. First of all, we believed that manufacturability is a fundamental concern and, because of that, all of our designs were tested against the coherence vector simulation mode of QCADesigner. To the best of all knowledge, all other reversible ALU's implementations used the bistable simulation mode, which lacks realistic considerations about quantum-mechanical characteristics of the device. This is a very important contribution of our work.

Another relevant issue in QCA designs is the way we cross wires. We chose the multi-layer strategy to crossing wires. In this approach the circuits could be constructed by stacking the cells in layers one above the other, that is, in multiple layers. According to this technique, the upper layers transport the information and, as a result, interlayer interference effects are suppressed and interaction between regular cells is strengthened. It's also easier to change the circuit for accommodate other crossing styles.

The challenging task to synchronize all signals along the circuit's datapath is also relevant to report. First we divided the longest path with the minimum number of clocking zones required for synchronization and correct thermodynamic operation. Then all other paths were segment to fit the same number of clocking zones.

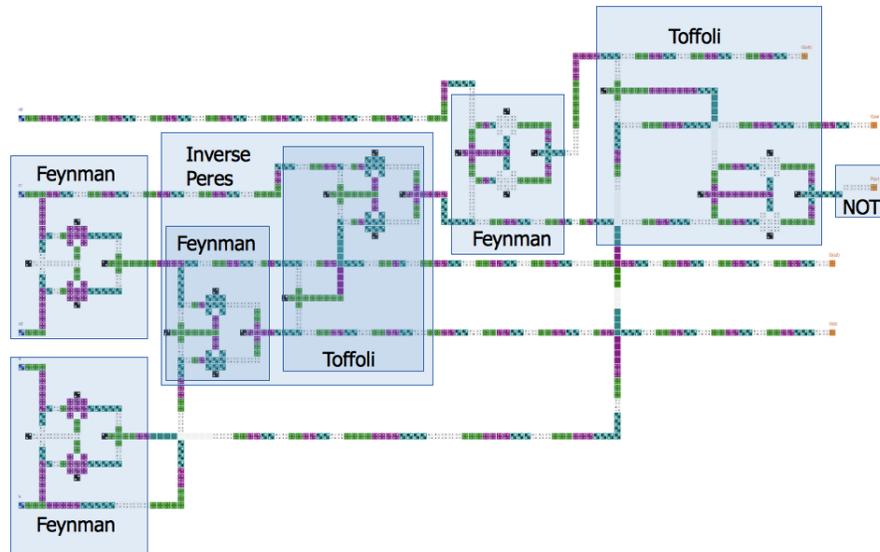


Fig. 4. Gupta's ALU QCA realization.

Another fundamental point to mention is our choice to build an ALU already proposed in literature instead of create our own. We made this choice because RevLib [13] is the resource for benchmarks within the domain of reversible and quantum circuit design. So, we will be able to compare our future designs with those of benchmarks as soon as these alternative implementations appear.

## VI. CONCLUSION

In this work, we proposed and implemented different reversible gates and an ALU in QCA nanotechnology. QCA is a promising nanoscale technology where components are nanosized and present clock rate on terahertz range. By combining the ultra-low power consumption of QCA and reversible computing, we believe that the proposed gates and circuits will approach the physical limits of possible electronic circuits.

We discussed about the design choices and performance implications along the construction of different QCA reversible gates and an Arithmetic Logic Unit. We demonstrate the functionality, test and validate the proposed architectures using QCADesigner simulator in a realistic mode.

For further research, we intend to build a library of reversible gates and circuits in QCA, which is essential for a technology mapping synthesis approach. There is a lot of other possible automatization in our QCA workflow as the synchronization issue solution, for example. We also envision to calculating the energy dissipation involved in different QCA implementations, such as molecular and magnetic.

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## REFERENCES

- [1] R. K. Cavin, P. Lugli, and V. V. Zhirmov, "Science and engineering beyond moore's law," *Proceedings of the IEEE*, vol. 100, no. 13, pp. 1720–1749, 2012.

- [2] C. S. Lent, P. D. Tougaw, W. Porod, and G. H. Bernstein, "Quantum cellular automata," *Nanotechnology*, vol. 4, pp. 49–57, 1993.
- [3] R. Landauer, "Irreversibility and heat generation in the computing process," *IBM journal of research and development*, vol. 5, no. 3, pp. 183–191, 1961.
- [4] A. Béruit, A. Arakelyan, A. Petrosyan, S. Ciliberto, R. Dillenschneider, and E. Lutz, "Experimental verification of landauer's principle linking information and thermodynamics," *Nature*, vol. 483, no. 7388, pp. 187–189, 2012.
- [5] E. Fredkin and T. Toffoli, "Conservative logic," *International Journal of Theoretical Physics*, vol. 21, no. 3, pp. 219–253, 1982.
- [6] J. Timler and C. S. Lent, "Maxwell's demon and quantum-dot cellular automata," *Journal of Applied Physics*, vol. 94, no. 2, pp. 1050–1060, 2003.
- [7] C. S. Lent, M. Liu, and Y. Lu, "Bennett clocking of quantum-dot cellular automata and the limits to binary logic scaling," *Nanotechnology*, vol. 17, no. 16, p. 4240, 2006.
- [8] M. Ottavi, S. Pontarelli, E. P. DeBenedictis, A. Salsano, S. Frost-Murphy, P. M. Kogge, and F. Lombardi, "Partially reversible pipelined qca circuits: combining low power with high throughput," *Nanotechnology, IEEE Transactions on*, vol. 10, no. 6, pp. 1383–1393, 2011.
- [9] H. Thapliyal and N. Ranganathan, "Reversible logic-based concurrently testable latches for molecular qca," *Nanotechnology, IEEE Transactions on*, vol. 9, no. 1, pp. 62–69, 2010.
- [10] B. Sen, M. Dutta, M. Goswami, and B. K. Sikdar, "Modular design of testable reversible alu by qca multiplexer with increase in programmability," *Microelectronics Journal*, 2014.
- [11] R. Devadoss, K. Paul, and M. Balakrishnan, "p-qca: A tiled programmable fabric architecture using molecular quantum-dot cellular automata," *ACM Journal on Emerging Technologies in Computing Systems (JETC)*, vol. 7, no. 3, p. 13, 2011.
- [12] L. H. Sardinha, A. M. Costa, O. P. V. Neto, L. F. Vieira, and M. A. Vieira, "Nanorouter: A quantum-dot cellular automata design," *Selected Areas in Communications, IEEE Journal on*, vol. 31, no. 12, pp. 825–834, 2013.
- [13] R. Wille, D. Große, L. Teuber, G. W. Dueck, and R. Drechsler, "RevLib: An online resource for reversible functions and reversible circuits," in *Int'l Symp. on Multi-Valued Logic*, 2008, pp. 220–225, RevLib is available at <http://www.revlib.org>.
- [14] P. Gupta, A. Agrawal, and N. Jha, "An algorithm for synthesis of reversible logic circuits," *IEEE Trans. on CAD*, vol. 25, no. 11, pp. 2317–2330, 2006.