Design and Implementation of Arithmetic Logic Unit (ALU) using Modified Novel Bit Adder in QCA

Kanimozhi.V [1]
P.G. Scholar - M.E.VLSI Design,
Kalaignar Karunanidhi Institute of
Technology,Coimbatore, India
kanivaratharaj27@gmail.com

Gowri Shankar.R [2]
Professor and Head - Dept of Electronics and
Communication Engineering,
Kalaignar Karunanidhi Institute of
Technology,Coimbatore, India
rgowri2000@gmail.com

Abstract—**Moore's law states that the number of transistors that could be integrated into a single die would grow exponentially with time. Thus this causes increasing computational complexity of the chip and physical limitations of devices such as power consumption, interconnect will become very difficult. According to recent analysis the minimum limit for transistor size may be reached. Thus, it may not be possible to continue the rule of Moore's law and doubling the clock rate for every three years. So in order to overcome this physical limit of CMOS-VLSI design an alternative approach is Quantum dot Cellular Automata (QCA). In ALU adder plays a vital role. In this survey a binary adder is taken for analysis and a new adder is designed based upon QCA technology. This modified novel bit adder is implemented into ALU structure. The aim of this proposed technique is that to reducing number of majority gates used in the design. This will lead to reduce number of QCA cells so that total area of ALU circuit can be minimized compare to previous designs. It also achieves reduced power consumption and high speed performances than all other existing ALU design which uses normal full adder..**

Index Terms—**Moore's law, CMOS, Area, power consumption, Quantum dot Cellular Automata (QCA), Full adder, ALU.**

I. INTRODUCTION

A. CMOS Technology

Microprocessor manufacturing processes was governed by Moore's law, and consequently microprocessor performance till now. Today many integrated circuits are manufactured at 0.25-0.33 micron processes. But recent studies indicate that as early as 2010, the physical limits of transistor sizing may be reached [2]. However the performance of various circuits in current CMOS-based architectures is close to reaching the limit. If the feature size of transistors is further reduced to a nanometer, it will produce quantum effects such as tunneling. Further, during device scaling process due to the effects of wire resistance and capacitance, the interconnections never scale automatically.

Addition is an essential operation in any Digital, Analog, or Control system [9]-[12]. Fast and accurate operation of all digital system depends on the performance of adders .The main function of adder is to speed up the addition of partial products generated during multiplication operation. Hence improving the speed by reduction in area is the main area of research in VLSI system design.

B. An Introduction to QCA Technology

As an alternative to CMOS-VLSI, an approach called the quantum cellular automata (QCA) is developed in 1993[1] to computing with quantum dots. Unlike conventional computers in which information is transferred from one place to another by electrical current, QCA transfers information by means of propagating a polarization state from one cell to another cell [7].The charge distribution in each cell is aligned along one of two perpendicular axes, so that the binary information can be encoded by using the state of the cell.

Tree adder is an alternate to conventional adder,because by using tree structure carries are generated in parallel and fast computation is obtained at the expense of increased area so power usage is also increased.. The main advantage of this design is that the carry tree reduces the number of logic levels

(N) by generating the carries in parallel.The parallel-prefix tree adders are more favorable in terms of speed due to the complexity O(log2N) delay through the carry path compared to that of other adders[6].

C. 1 Bit ALU Architecture

The Arithmetic Logic Unit (ALU) performs the basic arithmetic and logical operation.The ALU consists of arithmetic extender, logical extender and a full adder which is shown in Fig. 1.Three control signals will decides the operation of the ALU. M is the mode control variable which select between arithmetic and logical operations. S1 and S0 are selection line used in combination with M to select between the eight arithmetic and logical operation the ALU supports.Detail about Arithmetic and Logical extender is explained in [8].
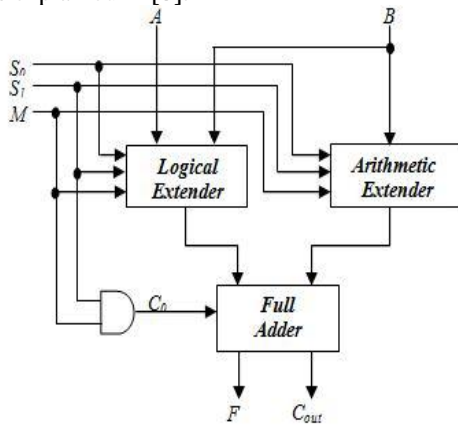

Fig 1: Architecture of ALU

The rest of this brief is organized as follows: A brief introduction to the QCA technology is discussed in Section II and existing adders designed using QCA is given in Section III, the novel adder design is then introduced in Section IV, simulation and comparison results are presented in Section V finally, in Section VI conclusions are drawn.

II BACKGROUND

A. Basics of QCA

The basic element of QCA technique is QCA cell. In QCA cell each cell is having four quantum dots [3] and in which two are free electrons. Fig.2 shows the QCA cell diagram. A quantum-dot cellular automata (QCA) cell is a square nanostructure of electron wells. The four dots are located in the four corners of this square structure.

The cell can be charged by using free electrons, because external power supply is not provided here. The electrons tunnel to proper location by using the clocking mechanism during the clock transition. Thus there exist two electrons in the QCA cell as shown in Fig. 2 and location of the electrons in the QCA cell is to represent the binary states. These two arrangements are representing logic 1 and logic 0 respectively by using which the binary information can be encoded.
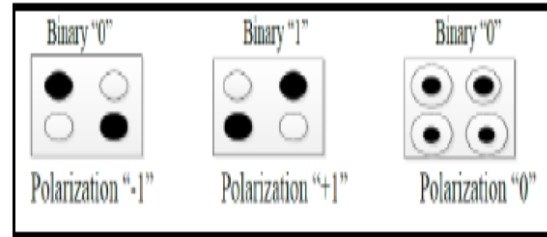

Fig 2: QCA Cell Polarization

. Majority gate and Inverter are the universal logic elements in QCA by using which we can derive any logic circuits using coupled quantum dot cell. Inverter is represented in Fig. 3 and Majority gate is in Fig. 4.
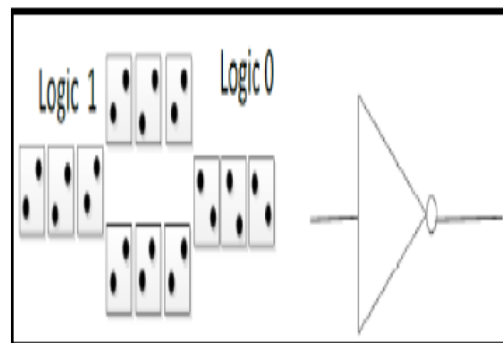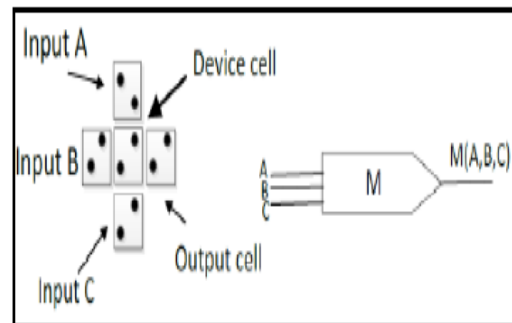

Fig 3: inverter

Fig 4: majority gate

In QCA design two types of crossover is possible such as termed coplanar crossover and multilayer crossover respectively.

III EXISTING QCA ADDERS

Several designs of adders in QCA are existing. The RCA [9], [11] and the CFA [10] process n-bit operands by cascading of n full-adders (FAs). A CLA architecture formed by 4-bit slices was presented [9].n-bit CLA has a computational path composed of $7 + 4 \times (\log 4\ n)$ cascaded MGs and one inverter The parallel-prefix BKA [11] exploits more efficient basic CLA logic structures.Its main advantage over the previously described adders, the BKA can achieve lower computational delay. When n-bit operands are processed, its worst case computational path consists of $4 \times \log 2\ n - 3$ cascaded MGs and one inverter. With the main objective tradeoff between area and delay, the hybrid adder (HYBA) described in [12] combines a parallel-prefix adder with the RCA. For n-bit operands, this architecture has a worst computational path consisting of $2 \times \log 2\ n + 2$ cascaded MGs and one inverter. When the methodology proposed in [13] was exploited, the worst case path of the CLA is reduced to $4 \times (\log 4\ n) + 2 \times (\log 4\ n) - 1$ MGs and one inverter. This approach can also be applied to design the BKA. In this case the overall area is reduced with respect to [11], but maintaining the same computational path. By applying the decomposition method [14], the computational paths of the CLA and the CFA are reduced to $7 + 2\log 2\ (n/8)$ MGs and one inverter and to $(n/2) + 3$ MGs and one inverter, respectively.

Recently developed novel n bit adder [5] has separate structure for carry and sum generation. This adder has 5n-4 number of MG's and n inverters for n bit adders. one problem in this structure is it will not produce correct output for LSB bit combination of input(a0b0=01).for example for adding 2 numbers such as 2(10) and 3 (11) the actual output is 5(101)but this adder[5] will produce sum as 4(100).

IV.PROPOSED QCA ADDER

In this section, we propose a two new QCA addition algorithm and the corresponding two-bit QCA adder structure that reduces the number of the majority gates and inverters required for existing designs[5] and eliminate above mentioned drawback also.

A. Modified Novel Bitadder 1

To introduce proposed Modified novel bitadder 1 - n bit architecture first it is designed a 2 bit basic module based on proposed algorithm. let us consider 2 operands such as A=a1a0 and B=b1b0 and we designed proposed 2bit module as shown in fig 5(a).For each bit the carry is generated by using one majority gate. Sum is calculated by cascading of 3 MG's.

Given three inputs a, b, and c, the MG performs the logic function reported in (1). provided that all input cells are associated to the same clock signal clk_x (with x ranging from 0 to 3)

$$M\ (a,b,c)=a.b+b.c+c.a \qquad (1)$$

To create an n-bit adder, let consider two n-bit addends $A = a_{n-1}, \ldots, a_0$ and $B = b_{n-1}, \ldots, b_0$ and for $i = n - 1, \ldots, 0$ and we arrange n proposed one-bit adders vertically in a column which is shown in fig5(b) and (c)respectively.
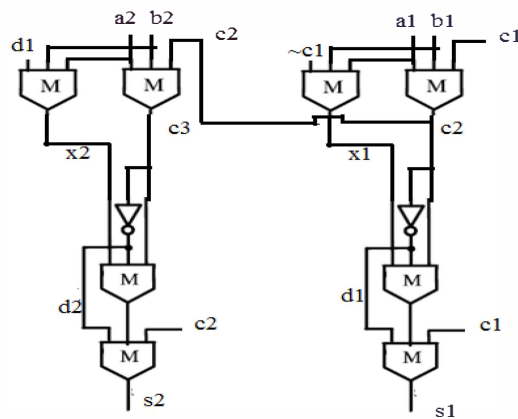
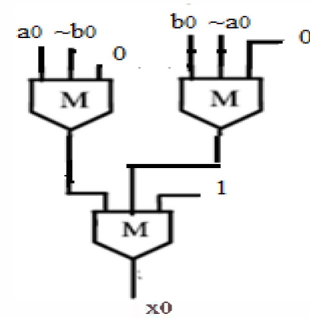

Fig 5(a): Modified novel bit adder 1: 2 bit basic module.

Fig 5(b): Modified novel bit adder 1- Calculation of x0

This proposed architecture can be implemented by using equation (2) and (3)

$$C_{i+1}= M\ (a_i, b_i, c_i) \tag{2}$$
$$S_i=M\ (M\ (M\ (a_i,\ b_i,\ d_{i-1}),\ M\ (a_i,b_i,c_i),\ d_i),\ d_i,\ c_i) \tag{3}$$
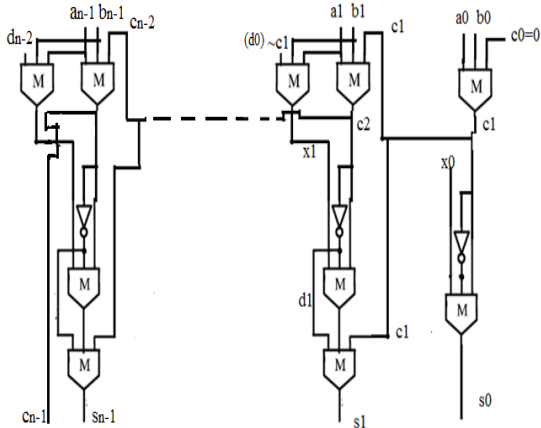Where $d_i = \sim c_{i+1}$

Fig 5(c): Modified novel bit adder 1: n bit basic module

The proposed n bit QCA adder consists of 4n+1 number of majority gates and n+2 inverters. It results in reduced hardware compared to the existing [5] structure and retains the simple clocking scheme.

B. Modified Novel Bit Adder 2

Here we now introduce a new Modified novel bit adder 2- n bit adder architecture which reduces hardware complexity compared to existing[5] and Modified novel bit adder 1 structure.The basic 2bit module for Modified novel bit adder 2 is shown in fig6(a).Here the carry is calculated in same way as in proposed 1 structure and sum block is modified which requires two majority gates only.

This proposed architecture can be implemented by using equation (4) and (5)
$$C_{i+1}= M\ (a_i, b_i, c_i) \tag{4}$$
$$S_i=M\ (M\ (a_i,\ b_i,\ d_{i-1}),\ d_i,\ ci_{-1}) \tag{5}$$
Where $d_i = \sim c_{i+1}$

To create an n-bit adder, let consider two *n*-bit addends $A = an-1, \ldots, a0$ and $B = bn-1, \ldots, b0$ and for $i = n - 1, \ldots, 0$ and we arrange n proposed one-bit adders vertically in a column which is shown in fig 6(b).
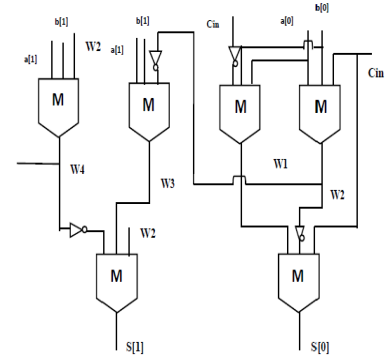

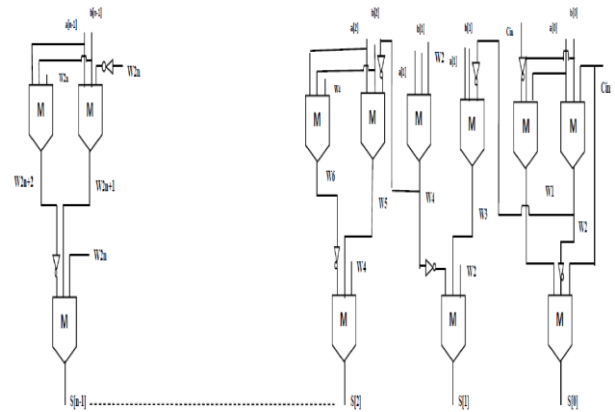Fig 6(a): Modified novel bitadder 2: 2bit basic module

Fig 6(b): Modified novel bit adder 2: n bit adder

The proposed n bit QCA adder consists of 3n number of majority gates and n inverters. It results in reduced hardware compared to the existing [5] structure and proretains the simple clocking scheme.

V SIMULATION AND SYNTHESIS RESULTS

Simulation is performed by using modelsim6.4a simulation tool and the operation is checked for all the input combinations.Fig 7 shows the drawback of existing[5] adder ie.,wrong output for LSB combinations of 01.
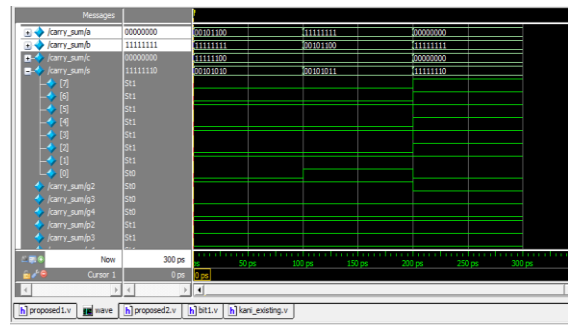

Fig 7: simulation result of existing adder[5]

A.Modified Novel Bit Adder

Fig 8(a) and 8(b) shows the simulation result of modified novel bit adder 1 and 2 respectively.
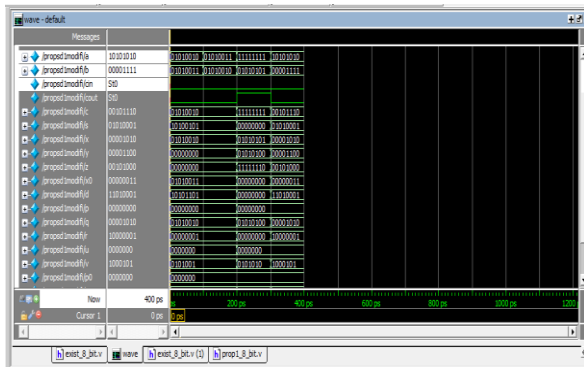

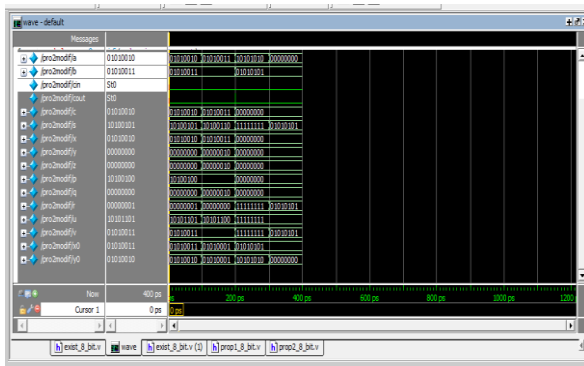Fig 8(a): simulation result of Modified novel bit adder 1

Fig 8(b): simulation result of Modified novel bit adder 2

Synthesis is performed by using xilnx ISE 8.1i tool fig 9(a) and fig 9(b) shows the area report of Modified novel bit adder 1 and Modified novel bit adder 2 respectively.Gate count comparision is shown in Table 1.
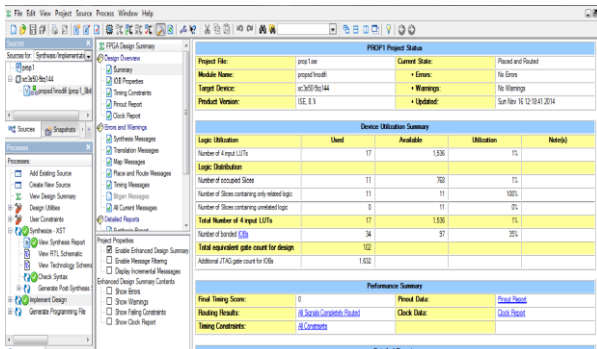

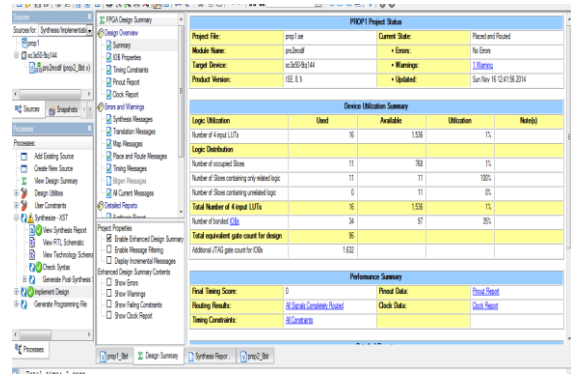Fig 9(a): Area report of Modified novel bit adder **1**

Fig 9(b): Area report of Modified novel bit adder 2

TABLE 1: COMPARISION FOR GATE COUNTS IN ADDERS

	Existing Adder	Modified Novel Bit Adder 1	Modified Novel Bit Adder 2
Gate Count (Xilinx)(8 bit)	141	102	96

B. Alu Design Using Modified Novel Bit Adder 2

Based on above discussion ,modified novel bit adder 2 is the best choice interms of area and delay.so one bit ALU is designed using Modified novel bit adder 2 .simulation and area ,delay result for proposed ALU is shown in Fig 10(a),Fig 10(b), Fig 10(c) respectively.It achieves less area and delay compared to existing ALU[8].
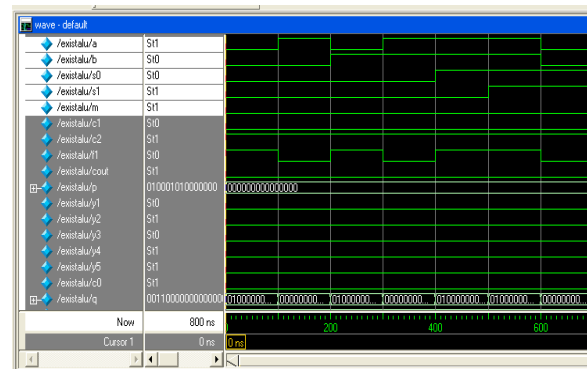

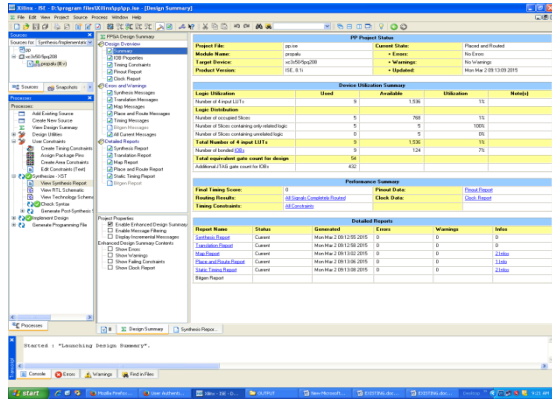Fig 10(a): Simulation result of proposed ALU
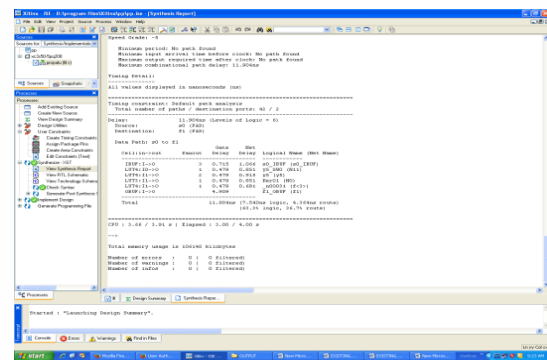
Fig 10(b): Area report of proposed ALU

Fig 10(c): Delay report of proposed ALU

VI CONCLUSION

A new adder in QCA technology was designed which achieves reduced area than all the existing QCA adders [5]. The Proposed modified novel bit adder 2 is implemented in 1 bit ALU circuit to improve the efficiency.The proposed ALU has total gate count of 54 which is reduced than existing ALU [8] in which gate count is 66.The delay required for proposed ALU structure is 11.904ns which is less than existing in which 15.433ns is needed.The functionality is checked by using modelsim simulation tool The Future extension of our work is to design 4 bit ALU in QCA using Modified novel bit adder 2 structure.

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