Design of high speed multiplier using Modified Booth Algorithm with hybrid carry look-ahead adder

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***Abstract*---** **In this paper novel method for multiplier and accumulator is proposed by combining reversible logic functions and hybrid carry look-ahead adder. Modified booth algorithm produces less delay in comparison with a normal multiplication process and it also moderates the number of partial products. The Carry look-ahead adder is used for controlling the overall MAC delay. The main purpose of designing a reversible logic is to reduce the circuit complexity, power consumption and loss of information. Here we survey on possible ways to make a full adder design using different reversible logic gates. We also proposed a new hybrid CLA from the existing hierarchical CLA which exhibits high performance in terms of computation, power consumption and area. Area, delay and power complexities of the resulting design are reported. The proposed MAC shows better performance compare to conventional method and has advantages of reduced area overhead and critical path delay. This new high speed hybrid carry look-ahead adders are simulated and synthesized using Synopsys (90 nm) Design Compiler and Xilinx ISE simulator.**

Keywords: Multiplier and accumulator (MAC), modified booth algorithm (MBA), Hybrid carry look-ahead adder (CLA), reversible logic gate (RLG), ripple carry adder (RCA).

I. INTRODUCTION

The advance development in the field of microelectronic makes it efficiently to use input energy to scramble the data more effectively and to transfer the data faster [5]. In many of these expertises are developed based on low power consumption in order to meet the desired applications. Multiplier is a very basic arithmetic logical unit and is used abundantly in circuits. Convolution, filtering and inner products are the vital processes of digital signal processing which uses the MAC application [4]-[6]. Discrete wavelet transform or discrete cosine transform are the broadly used DSP methods which are not linear functions in nature. This is because they are principally done by repetitive application of addition and multiplication which determine the execution performance and speed of the entire calculation. The modified booth's algorithm (MBA) [1]-[2] is usually used for high speed multiplication.

In general, the multiplier consists of three parts primarily: A tree to compact the partial products, Booth encoder and the final adder. A Wallace tree is simply a logical function which is used for the addition of the partial products. The processing speed of a multiplier can be increased by reducing the amount of the partial products. To achieve the above intended aspect, MBA [1] algorithm is hired mostly where Wallace tree improves the speed with which the partial products are added [4]-[8]. Many parallel multiplication architectures have been explored in order to improve the speed of the MBA algorithm. Therefore, this has been employed to various digital filtering calculations.

Reversible logic is the recent advancement in the electronics field as it shows low heat dissipating features. It has been proven that reversible gates can be used to realize any Boolean function [3]. That is whenever a high speed process happens there

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will be loss of information or data which will be dissipated in the form of heat. In this design we used RLG as substitutes for normal FAs in order to decrease the delay and power. A reversible logic circuit should possess properties like usage of less number of garbage outputs, usage of less number of gates [3], and usage of less constant inputs. In MAC units, conventional CLA is used for reducing the number of bits in the final addition and control the overall MAC unit delay.

In this paper, we have discussed a novel design for a Multiplier using improvised Booth Algorithm by Reversible Gate Logic and also substituting the conventional CLA with hybrid CLA Section II discusses overview of CLA. Section III discusses overview of proposed CLA. Section IV introduces reversible logic gate function. Section V overview of proposed MAC and architecture of CSA tree. Section VI provides the implementation. Section VII is the conclusion.

II. OVERVIEW OF CONVENTIONAL CLA

RCA has an extensive circuit delay because of many gates being used in the carry path from LSB to MSB [9]. So we use alternate design, Carry Look-ahead Adder. CLA is a high speed addition process. The implementation of parallel adder was introduced in CLA to attain high speed process. Generally it is used for addition of N-bit numbers in fast manner. Delay of the addition process depends mainly on the size of the operands. Here generating (G) and propagating (P) concepts are used to generate carries.

$G_i = A_i \& B_i$

$P_i = A_i \oplus B_i$

$Sum_i = C_i \oplus P_i$

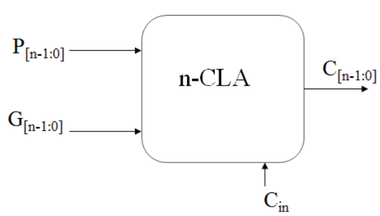

Fig. 1.n-bit CLA module

The n-bit CLA module accepts n-bit signals P[n-1 : 0] and G[n-1 : 0] and the carry-in signal (C_{in}) produces n+1-bit carry signals C[n : 0], according to the equations (1),(2),(3) the carry value depends upon the number of input bits.

$C_1 = C_0P_0 + G_0$ (1)

$C_2 = C_0P_0\,P_1 + P_1G_0 + G_1$(2)

$C_3 = C_0P_0\,P_1P_2 + P_1\,P_2\,G_0 + G_1\,P_2 + G_2$(3)

...

$$C_{n-1} = C_{in} \cdot \prod_{i=0}^{n-2} P_i + \sum_{i=0}^{n-2} G_i \cdot \prod_{j=i+1}^{n-2} P_j$$

We can write the carry at bit i as,

$$C_i = C_{in} \prod_{j=0}^{i-1} P_i + \sum_{J=0}^{I-1} G_i \cdot \prod_{k=j+1}^{i-1} P_k \,, \qquad 0 \le i \le n$$

These are the steps and equations taken for addition process using Conventional Carry Look-ahead Adder.

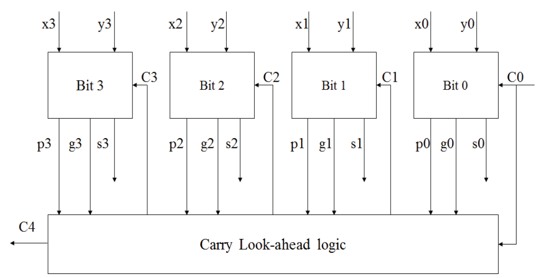

Fig. 2. 4-bit Conventional CLA

III. PROPOSED CLA DESIGN

In this section, we discuss the proposed method of hybrid carry look-ahead adder. This method is divided into three stages as like hierarchical carry look-ahead adder. The Fig. 3 show the design of Hybrid CLA.

In stage one, accept the two n-bit number of inputs and produce propagate and generator value. After finishing this stage, we move to next stage. In this stage we generate the intermediate carry and the overall carry is also generated. Now carry has to be generated from the top module becauseit occupy more space. One more advantage is that there is no need to generate the carry propagate (Pout) and carry generate (Gout) signals. Here the carry of the whole design is generated in the bottom stage of the structure. Simultaneously we can generate the sum of every bit. By this method the area of the design is reduced. So this is one way to design high speed and less area carry look-ahead adder design.

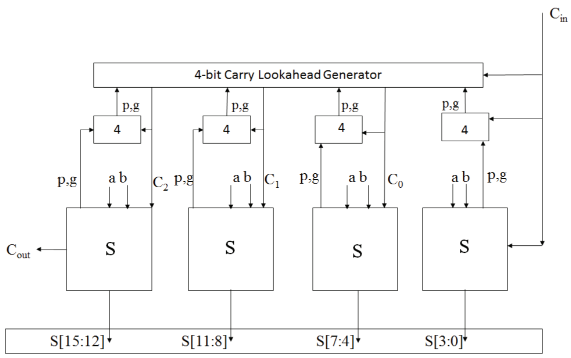

Fig. 3. Hybrid CLA for 16-bit

P: an indicator whether the carry was propagated to the component. In other words, the carry is propagated through the entire component if and only if it was propagated through every one of the components from the previous stage. The equation (4) is for the 4-bit module.

$$P = \prod_{i=0}^{n-1} P_i$$

$$P = P_0 P_1 P_2 P_3 \quad (4)$$

G: an indicator whether the carry was generated to the component. In other words, the carry is generated through the entire component if and only if it was generated through every one of the components from the previous stage. The equation (5) is for the 4-bit module.

$$G = \sum_{i=0}^{n-1} G_i \cdot \prod_{j=i+1}^{n-1} P_j$$

$$G = P_1 P_2 P_3 G_0 + G_1 P_2 P_3 + G_2 P_3 + G_3 \qquad (5)$$

Note that the $\sum -$ components can also be considered as “carry generators” since they produce the carry-propagated and carry-generated indicators.

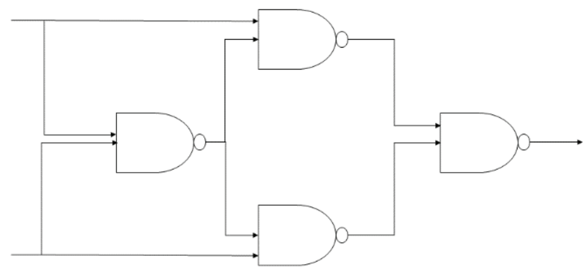

Fig. 4. Constructing 2-input XOR gate using 2-input NAND gates

The main difference is in designing the overall structure using NAND gate. According to the analysis, NAND gate is better than all other gates because it has lesser area and less delay and it consume less power over NOR gate. Instead of 2-input XOR gate, we can use four 2-input NAND gate to get the same result. The design using four 2-input NAND gate instead of 2-input XOR gate is shown in fig. 4.

IV. OVERVIEW OF REVERSIBLE LOGIC GATES

Now a days, energy dissipation is the major issue in many applications. In every logical operation heat is dissipated from the circuit. This mean loss of information happening in the circuit. In all high speed designs heat dissipation occurs. Recently several researchers have focused to reduce the loss of information from the circuit by using reversible logic gates design. It is one of the best design to control the loss of information and it takes less power. The purpose of designing a reversible logic is to decrease the cost, reduce the loss of information and power and reduce the garbage output. Reversible logic function is used to determine the input from the output. Power dissipation is also very less, because of using reversible logic gates. It controls the overall power dissipation. Reversible logic is used in quantum computation, nanotechnology and other low power digital circuits[3]. The essential gates used for reversible logic synthesis are New Gate, Feynman Gate and Toffoli gate.

One bit of information loss, dissipates

k T ln 2 Joules of energy

Where, k is Boltzmann's constant and T is absolute temperature.For room temperature, energy loss is small for one bit, 2.9×10^{-21} J

The main function of reversible logic is the number of inputs are equal to number of outputs. A device is said to be deterministic if its inputs and outputs be individually retrievable from each other. In other words such a device can also be called logically reversible. If the whole device has the capacity to run backward it can be called physical reversible. These are the two basic conditions for reversible logic. Sometimes we get garbage outputs for attaining number of inputs equal to number of outputs. So garbage outputs are additional to make inputs and outputs equal whenever necessary.

Input + constant input = output + garbage

Feynman gate, New gate and Toffoli gate from these three gates, we can design a new full adder circuit. These different reversible full adder design are used in many arithmetic calculations like multiplication.

A. Feynman Gate

The Feynman gate has two inputs, one output and one garbage output. The inputs named as input vector I_v (A,B) and output is named as output vector O_v (A, A⊕B). It is also called 2*2 Feynman gate. The block diagram for Feynman gate is shown in the fig.5.

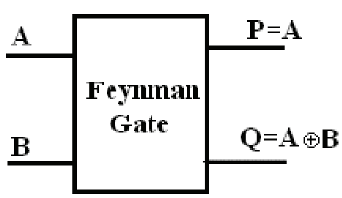

Fig. 5.Block diagram

B. Toffoli gate

The Toffoli gate has three inputs, one output and two garbage outputs. The inputs named as input vector I_v (A,B,C) and output is named as output vector O_v (A, B, AB⊕C). It is also called 3*3 Toffoli gate. The block diagram for Toffoli gate is shown in the fig.6

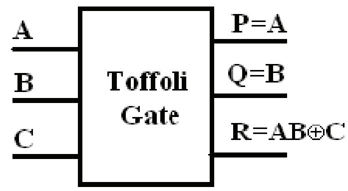

Fig. 6.Block diagram

C. New Gate (NG)

The New gate has three inputs, two outputs and one garbage output. The inputs named as input vector I_v (A,B,C) and output is named as output vector O_v (A, AB⊕C, A'C'⊕B'). It is also called 3*3 New gate. The block diagram for new gate is shown in the fig.7.

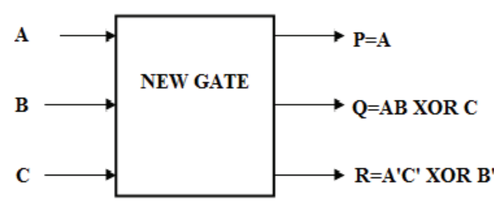

Fig. 7. Block diagram

V. PROPOSED MAC DESIGN

This section examines the proposed design and address how delay can be reduced effectively. This in turn moderates number of partial product rows which are used in order to reduce the number of multiplication in such a way that it improves the speed. Therefore we proposed a novel area efficient and high speed MAC architecture which is an improvement over the current conventional Architecture. The results of accumulation and multiplication stages clubbed using hybrid reduction through HA, FA and CLA. This helps us to attain more efficiency and speed. In addition, the normal full adder in the CSA is replaced by a new reversible logic gate. The circuit is simulated using Verilog HDL and synthesized in Xilinx ISE Simulator. We anticipate the proposed MAC can be used in high speed DSP application. In Fig.8 the proposed structural design has been demonstrated and it contains a Booth encoder, CSA and the final addition stage. The tree contains the reversible logic gates that had replaced the normal FAs which improve the delay of the adder. Here also we use hybrid CLA in place of conventional CLA to add the sum [S] and carry [C].The structural design of the hybrid CSA has been shown in Fig.9, which performs 8X8-bit operation. It was developed based on the existing architecture. In Fig.8, Sum[i] and Carry[i] are corresponding to the i^{th} bit of the feedback sum and carry. Z[i] is the i^{th} bit of the sum of the lower bits for each partial product that were added in advance. Since the multiplier is for 8 bits, totally four partial products ($Q_0[7:0]$~$Q_3[7:0]$) are generated from the Booth encoder.

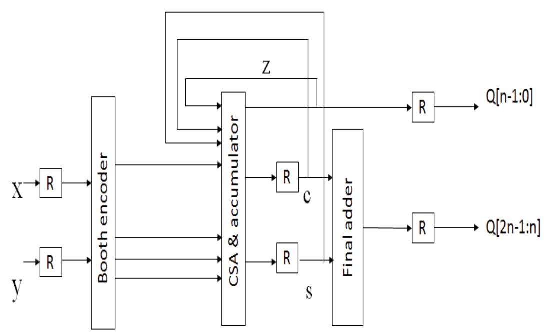

Fig.8.Parallel MAC unit based on MBA [1]

This CSA needs a minimum of four rows of reversible logic FA for the four partial products. Thus for accumulation of previous result, one more level of row is needed along with the previous ones. The grey square in Fig. 9 represents a HA and the white square represents a reversible logic FA. The rectangular symbol with five inputs shows a 2-bit CLA with a carry input. The critical path of this CSA is decided by the 2-bit CLA. It is also possible to use FAs to implement the CSA without using CLA. Instead of this conventional CLAwe use a hybrid CLA to improve the performance. However, the number of bits in the final adder will be increased even if the lower bits of the earlierpartial products are not processed in advance by the CLA. So when the MACis considered, its performance is reduced. The proposed CSA structural design have been compared and briefed with the other existing architectures in Table I. The biggest differences between proposed and the others is that we used reversible full adder and hybrid carry look-ahead adder in place normal full adder and conventional CLA.

TABLE I

CHARACTERISTICS OF CSA

References	**[9]**	**[5]**	**[1]**	**Proposed method**
Accumulation	Result data of final addition	Result data of final addition	Sum and carry of CSA	Sum and carry of CSA
CSA tree	FA	FA, 2-bits CLA	FA, HA, 2-bits CLA	Reversible logic FA, HA and 2-bit hybrid CLA

VI. IMPLEMENTATION

In this section, the proposed MAC is implemented and analyzed. The results of proposed is compared with conventional design. And also we designed a new CLA and reversible logic full adder. The Synopsys tool (DC) Design Compiler (Synopsys Design Vision- CMOS 90nm technology) generates the area and power report of the proposed design of hybrid carry look-ahead adder.

TABLE II

Delay time analysis

Addition	**Conventional CLA**	**Proposed method(HYBRID CLA)**
4-BIT	8.92ns	8.29ns
8-BIT	13.16ns	12.81ns

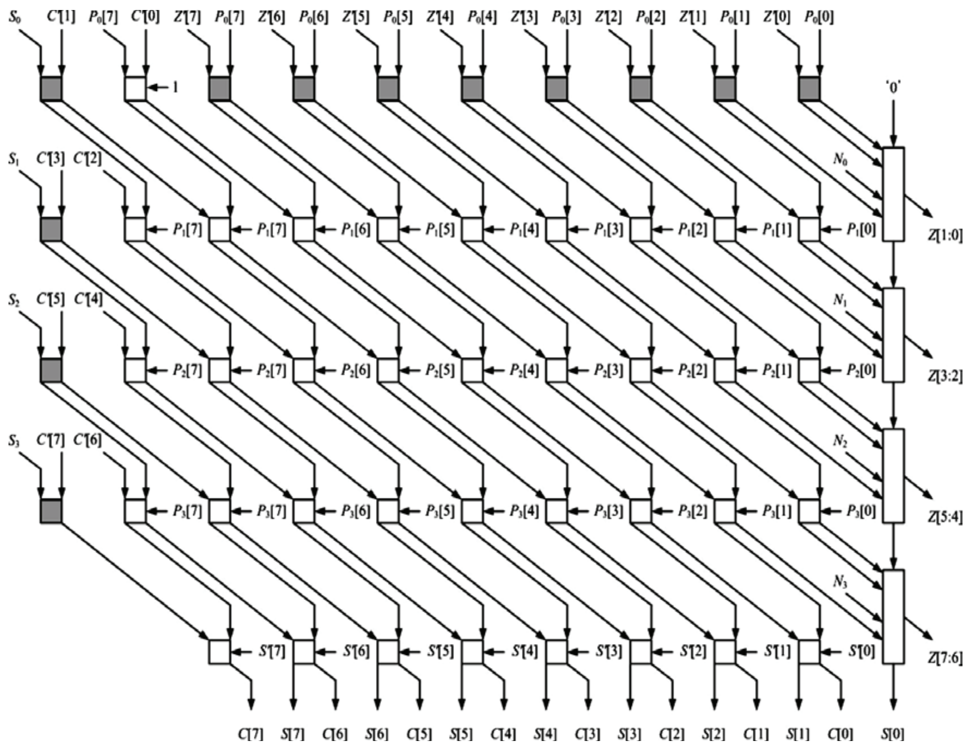

Fig.9. Architecture of CSA

The proposed architecture is compared with the conventional booth multiplier in Table IV. As it was difficult in comparing other factors we compared with only delay and area. The proposed MAC is synthesized by using Xilinx simulator. We achieved a delay of 27.31ns while the same in the previous work was 34.35ns, which means that we designed a high speed MAC. This improvement is mainly due to the use of Hybrid carry look-ahead adder and reversible logic.

TABLE III

Area and power report

4-bit addition	AREA(μm^2)	POWER(μW)
Conventional CLA	161.88	42.85
Proposed method HYBRID CLA	196.10	45.08

The architecture from the conventional method used normal full adder and had maximum delay. But in this proposed work, we achieved significant improvement in delay with little increase in power.

TABLE IV

Comparison table for MAC

Parameter	MBA [1]	Proposed MAC
No. of slices used	178 out of 4656	169 out of 4656
No. of LUT's	355 out of 9312	307 out of 9312
Total Delay	34.35ns	27.31ns

VII. CONCLUSION

In this paper, a new MAC structural design is proposed. The whole MAC shows has been improved by eradicating the liberated accumulation process that has the greatest delay, by substituting Conventional CLA with hybrid CLA. The proposed method of CLA has less combinational path delay when compared to existing CLA design. Here we presented a new full adder design using reversible logic gates. The reversible logic FA gates have less number of reversible gates and garbage output. So it takes very less power and there is no loss of data during the function. The proposed design of MAC was implemented and synthesized through Xilinx ISE tool. The proposed design can be used proficiently where we need a high speed of operations such as DSP. As of future work, the proposed CLA and Reversible logic full adder could be efficiently used in low power digital signal processing application, nanotechnology, MAC unit, filter, convolution, quantum computing, cryptography, DNA computing and computer graphics etc.

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