Primitive components of Reversible Logic Synthesis

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***Abstract*--- Reversible logic has various applications in fields of computer graphics, optical information processing, quantum computing, DNA computing, ultra low power CMOS design and communication. As our day to day life is demanding more and more portable electronic devices, challenging focus on technology is demanding great system performance without any compromise in power consumption. It is obvious to find tradeoff between processing power and heat generation. As decreased processing speed leads to reduced power consumption but obviously compromise in performance is not acceptable for sophisticated applications. Thus power consumption is a prime target now days. Needless to say, researchers will now look at reversible logic in this vein. Primitive component of reversible logic synthesis are reversible logic gates .Thus it is very important for a new researcher to look into extensive literature survey of reversible logic gates. Many papers have been reported with review of reversible logic gates. This paper aims on updates in reversible logic gates which are stepping stones in design and synthesis of any complex reversible logic based synthesis.**

***Keywords*-Reversible; Power consumption; Primitive component,; Optimization metrics**

I. INTRODUCTION

In 1961, R. Landauer [1] stated that "amount of energy dissipated for every bit erasure during an irreversible operation is given by KTln2 joules where K is Boltzmann's constant and T is the operating temperature. In 1973 C.H.Bennett [2] proposed the solution to R. Landauer statement and showed that KTln2 energy dissipation would not occur, if computation is done in a reversible manner since amount of energy dissipated in a system depends directly on numbers of bits erased during computation. Classical gates like two input AND, OR, NAND, NOR, XOR and XNOR are irreversible as we can't uniquely reconstruct input states from output states. Here two bit input state is mapped to one bit output state leads to erasure of one bit and consequently loss of energy. We can avoid this energy loss by mapping n bit input states to n bit output states so that input states can be uniquely recovered from output states and under such circumstances, a gate is said to be reversible. Quantum gates or reversible gates differ from Classical gates in a way that a) quantum gates work on qubits rather than bits b) feedbacks are not permitted in reversible logic circuits made with reversible logic gates so called acyclic and c) there is no fan out allowed means several copies of qubits are not allowed. It is very important to know that out of four 1*1 one qubit gates; only two are reversible i.e. trivial gate and not gate. Similarly out of 256 possible 2*2 two qubit gates; only 24 are reversible as shown in table 1.

II. NCV GATE LIBRARY

NCV gate library contains following set of quantum gates i.e. NOT gate, CNOT gate and controlled V and controlled V^+ gates. Controlled V and controlled V^+ gates are basically types of controlled square root of NOT gates. In both of these gates, when control input is 0 then second input is propagated as it is to output, Two V gates in series operation becomes CNOT gate or inverter. Similarly two V^+ gates activated in series operation becomes CNOT or inverter gate and one V and another V^+ gate in series operation become an Identity gate or buffer. Here block diagram of a 2*2 reversible gate is presented in Fig.1.1 with A and B as input and P and Q as output. Here quantum implementation of NOT gate, CNOT gate and Controlled V and controlled V^+ gates is given in Fig 1.2, Fig 1.3, Fig 1.4 and Fig 1.5 respectively .Quantum implementation of integrated qubit gates can be implemented by cascading quantum implementation of CNOT gate with controlled V gate or with controlled V^+ gate.

978-1-5090-0210-8/16 $31.00 © 2016 IEEE
DOI 10.1109/CICT.2016.134

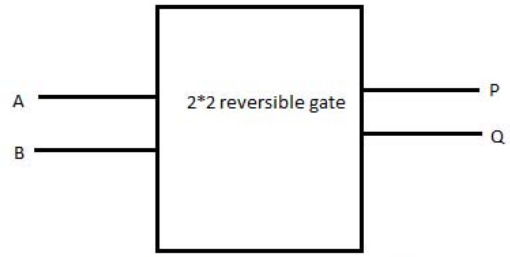


Fig 1.1:Block Diagram of 2*2 Reversible Gate

Fig 1.2 : Quantum Implementation of NOT gate

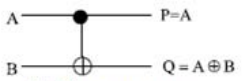


Fig 1.3 : Quantum Implementation of CNOT gate

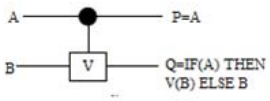


Fig 1.4 : Quantum Implementation of controlled V gate

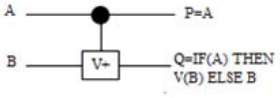


Fig 1.5: Quantum Implementation of controlled V^+ gate

Table1 represents all possible existing 24 2*2 reversible logic gates:-

Table 1: Representation of all possible existing 24 2*2 reversible logic gates

Reversible gate	P	Q	Reversible gate	P	Q	Reversible gate	P	Q	Reversible gate	P	Q
1	A	B	7	$\overline{A \oplus B}$	B	13(Feynman Gate)	A	$A \oplus B$	18	$\overline{A \oplus B}$	$\bar{B}$
2(Swap Gate)	B	A	8	B	$\bar{A}$	14	B	$A \oplus B$	20	$\overline{A \oplus B}$	$\bar{A}$
3	$A \oplus B$	B	9	$\bar{A}$	$\overline{A \oplus B}$	15	$A \oplus B$	A	21	$\bar{A}$	B
4	A	$\overline{A \oplus B}$	10	$\bar{B}$	$\bar{A}$	16	$\bar{B}$	$\overline{A \oplus B}$	22	$\bar{A}$	$\bar{B}$
5	$\overline{A \oplus B}$	A	11	$A \oplus B$	$\bar{B}$	17	A	$\bar{B}$	23	$A \oplus B$	$\bar{A}$

III. MULTI QUBIT LOGIC GATES

There exist 16777216 different 3*3 three qubit gates however number of reversible 3*3 gates is much smaller i.e.40320.Here fundamental 3*3 Reversible logic gates and other popular 3*3 reversible logic gates are described in Table 2 and Table 3 respectively with their logic expression, quantum cost, special feature respectively. To justify quantum cost; Quantum implementation of logic gates is also given. Table 4 describes all popular 4*4 reversible logic gates and to justify quantum cost, quantum implementation is also given. Table 5 describes 5*5 reversible logic gates and to justify quantum cost, quantum implementation is also given.

Table 2: Fundamental 3*3 Reversible Logic gates

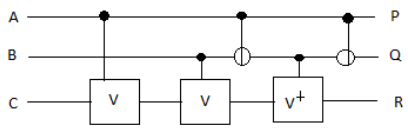
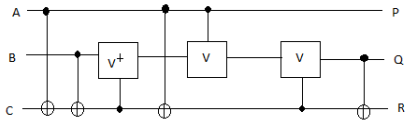
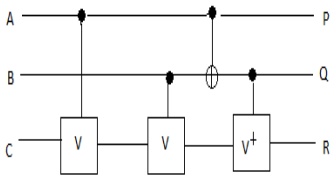
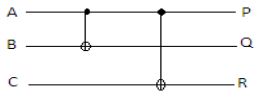
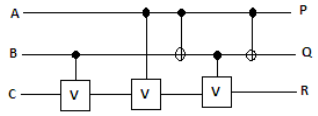
Reversible Logic Gate	*Specification*	*Expression*	*Quantum Cost*	*Feature*	*Quantum Implementation*
Toffoli/CCNOT Gate[3]	3*3	P = A Q = B R = AB⊕C	5	Universal Reversible Logic Gate	 Fig 1.6: Quantum Implementation of Toffoli Gate
Fredkin Gate/CSWAP Gate[4]	3*3	P = A Q = $\bar{A}$B⊕AC R = $\bar{A}$C⊕AB	5	Universal Reversible Logic Gate, Parity Preserving Reversible Logic Gate	 Fig 1.7: Quantum Implementation of Fredkin Gate
Peres Gate/NTG[5]	3*3	P = A Q = A⊕B R = AB⊕C	4	Lowest Quantum Cost	 Fig 1.8: Quantum Implementation of Peres Gate
Double Feynman Gate[6]	3*3	P = A Q = A⊕B R = A⊕C	2	Parity Preserving Reversible Logic Gate	 Fig 1.9: Quantum Implementation of double Feynman Gate

Table 3: Other popular 3*3 Reversible Logic Gates

Reversible Logic Gate	*Specification*	*Expression*	*Quantum Cost*	*Feature*	
BJN/MTG Gate[7]	3*3	P = A Q = B R = (A+ B)⊕C	5	Universal Logic Gate, Used for FAN OUT	 Fig 1.10: Quantum Implementation of BJN Gate

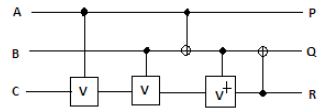
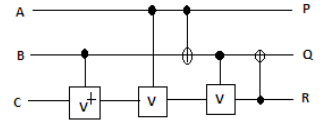
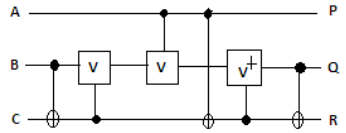
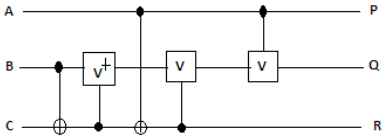
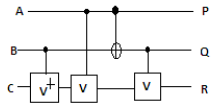
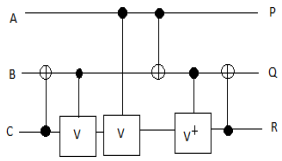
YAG/UPG Gate[8]	3*3	$P = A$ $Q = (A \oplus B) \oplus (AB \oplus C)$ $R = AB \oplus C$	4	AND,NAND,OR,NOR	 Fig 1.11: Quantum Implementation of UPG Gate
RC-I Gate[9]	3*3	$P = A$ $Q = \bar{A}B \oplus C$ $R = A\bar{B} \oplus C$	4	1 bit comparator	 Fig 1.12: Quantum Implementation of RC-I Gate
RMUX 1 Gate[10]	3*3	$P = A$ $Q = \bar{A}B + AC$ $R = \bar{A}C + A\bar{B}$	4	Multiplexer	 Fig 1.13: Quantum Implementation of RMUX1 Gate
RMUX2 Gate[10]	3*3	$P = A$ $Q = \bar{A}B + AC$ $R = (A \oplus B) \oplus C$	4	Multiplexer	 Fig 1.14: Quantum Implementation of RMUX2
TR Gate(TRG)[11]	3*3	$P = A$ $Q = A \oplus B$ $R = A\bar{B} \oplus C$	4	Subtractor	 Fig 1.15: Quantum Implementation of TR Gate
MFRG Gate[12]	3*3	$P = A$ $Q = A\bar{B} \oplus A\bar{C}$ $R = A\bar{C} \oplus AB$	4	Universal Logic Gate with reduced quantum cost	 Fig 1.16: Quantum Implementation of MFRG Gate

Table 4: Popular 4*4 Reversible Logic Gates

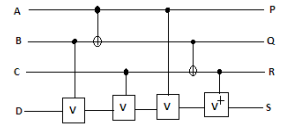
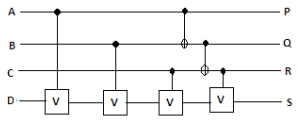
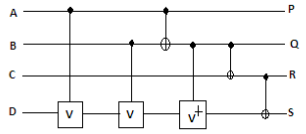
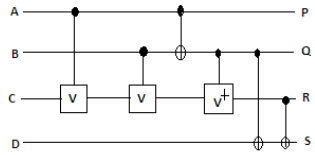
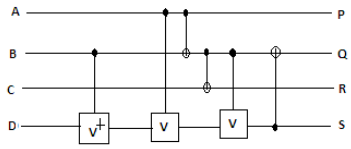
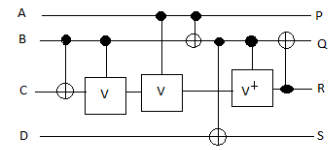
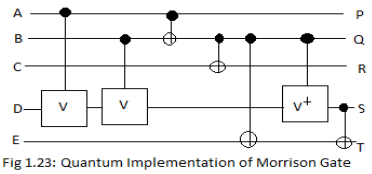
Reversible Logic Gate	Specification	Expression	Quantum Cost	Feature	
Double Peres/MTSG Gate/DPG/PFAG[13]	4*4	$P = A$ $Q = A \oplus B$ $R = A \oplus B \oplus C$ $S = (A \oplus B)C \oplus AB \oplus D$	6	Reversible Full Adder Gate	 Fig 1.17: Quantum Implementation of Double Peres Gate
HNG Gate[14]	4*4	$P = A$ $Q = B$ $R = (A \oplus B) \oplus C$ $S = (A \oplus B)C \oplus AB \oplus D$	6	Reversible Adder	 Fig 1.18: Quantum Implementation of HNG Gate
MRG Gate[15]	4*4	$P = A$ $Q = A \oplus B$ $R = A \oplus B \oplus C$ $S = (AB \oplus D) \oplus ((A \oplus B) \oplus C)$	6	OR,NOR,XOR,XNOR	 Fig 1.19: Quantum Implementation of MRG Gate
PAOG Gate[15]	4*4	$P = A$ $Q = A \oplus B$ $R = AB \oplus C$ $S = (AB \oplus C) \oplus ((A \oplus B) \oplus D)$	6	OR,NOR,AND,NAND	 Fig 1.20: Quantum Implementation of PAOG Gate
RC-II Gate[9]	4*4	$P = \bar{A}$ $Q = A\bar{B} \oplus D$ $R = A \oplus B \oplus C$ $S = A\bar{B} \oplus D$	5	Reversible sign bit comparator	 Fig 1.21: Quantum Implementation of RC-II Gate
RC Gate[15]	4*4	$P = A$ $Q = (A \oplus B) \oplus (B \oplus AB)$ $R = B \oplus C \oplus AB$ $S = A \oplus B \oplus D$	5	Comparator	 Fig 1.22: Quantum Implementation of RC Gate

Table 5: 5*5 Reversible Logic Gate

Reversible Logic Gate	Specification	Expression	Quantum Cost	Feature	
Morrison Gate[15]	5*5	$P = A$ $Q = A \oplus B$ $R = (A \oplus B) \oplus C$ $S = AB \oplus D$ $T = ((A \oplus B) \oplus E) \oplus (AB \oplus D)$	7	OR,AND	 Fig 1.23: Quantum Implementation of Morrison Gate

IV. CONCLUSION AND FUTURE SCOPE

This paper aims not only on updates in reversible logic gates with their expressions, special features and quantum cost but also on their quantum implementation to justify quantum cost which are stepping stones in design and synthesis of any complex reversible logic based synthesis. A new researcher may begin with basics of reversible logic gates and implement optimum reversible logic circuit based on various optimization metrics like ancillary inputs, garbage outputs, quantum cost.

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