Low Power High Speed Area Efficient Error Tolerant Adder Using Gate Diffusion Input Method

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Abstract–**In digital VLSI circuits, perfectly accurate outputs are not always needed. So designers have started to design error tolerance circuits which provide good enough output for computation. On the basis of this fact, error tolerant adder (ETA) is designed which provides a way to achieve good power and speed performance. In this paper, an emerging logic style of circuit design, gate diffusion input (GDI) technique is adopted to design a 32-bit ETA. The proposed design reduces area in terms of area the transistor count to a great extent as well as improves the delay and power performance. Simulation results have shown that proposed design achieves 38% improvement in the Power-Delay-Product when compared to the existing design.**

Keywords– *Adder, ETA, GDI, Power dissipation, VLSI.*

I. INTRODUCTION

Growing market of multimedia applications has boosted the need of low power portable devices. At the same time, high speed performance is also desirable. To achieve both of these goals simultaneously, designers have started to compromise with accuracy because perfectly accurate results are rarely needed and good enough outputs are sufficient for computation. This fact has led the concept of error tolerance which has been applied mainly in adders, known as Error Tolerant Adder (ETA). ETA has been designed to eliminate the need of carry propagation in addition operation because carry propagation from one stage to another consumes a lot of time which causes the slow operating speed of normal adders. By adopting this new concept, improvement in speed and power consumption has been achieved [1].

In the previous works, either the basic structure of ETA is altered or the logic style for hardware implementation is changed [2-5]. However, the delay and power performance are improved in these architectures but the industry demand of low power, faster adder is still increasing. So there is still a need of new ETA architecture that deals with these demands [6-8].

In this paper, we will discuss a new logic style based ETA which is more efficient than the already existing architectures. This proposed ETA is designed using GDI logic style which substantially reduces area in terms of the transistor count. Also the delay and power performance is also improved in this new design.

II. BASIC OPERATION OF ETA

In the basic structure of ETA [1], the operands are divided into two parts: accurate and inaccurate one. The length of each part can be equal or unequal depending on the requirement of accuracy and speed. We are considering 12 bits in accurate part and remaining 20 bits in inaccurate part. The addition process starts from the joining point of two parts and goes towards the two opposite direction simultaneously. Basic block diagram elaborating the concept of ETA addition arithmetic is shown in Fig.1.

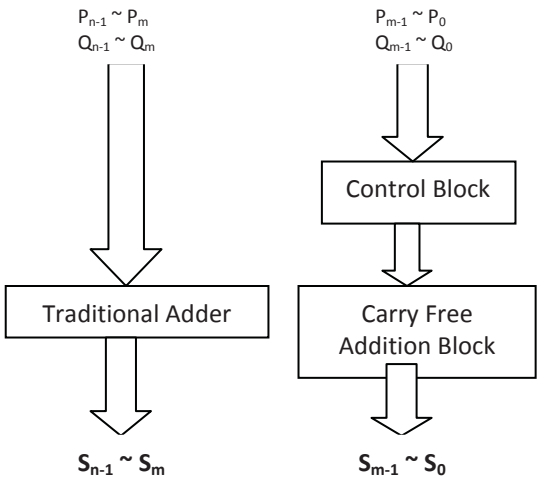

Fig.1. Basic Block Diagram of ETA

The accurate part can be designed by using any one of the available traditional adders like ripple carry adder, carry look ahead adder, carry bypass adder and etc. The inaccurate part is designed such as to eliminate the propagation of carry from one bit to next one. This part consists of two blocks: control block and carry free addition block. The control block checks all the bits fed to the inaccurate part and monitors when both incoming bits go high. The control block output at that position and that to the right of that position are then made high. A number of control logic generating cells (CL) are connected to form this control block.

In [2], the structure of control block is modified. The modified structure is shown in Fig.2. In this, the array of CLs which forms the control block is partitioned into smaller

blocks of equal size. The bits in a particular sub-block are bypassed by OR gates whenever a particular bit of control logic goes high, thus reducing overall delay of sum computation.

The carry free addition block consists of a chain of modified EXOR (MXOR) gates as shown in Fig.3, which generates a sum bit based on a control signal "CTL" which is obtained from aforesaid control block. When the value of this CTL signal is zero, the normal EXOR operation is performed over input bits. A logic high value of CTL signal sets the output to logic "1" irrespective of the value of input bits.

III. PROPOSED GDI BASED ETA ARCHITECTURE

A. Background of GDI Technique

The above mentioned architecture of ETA has been implemented using the conventional CMOS logic style. In our proposed architecture, gate diffusion input (GDI) method, is used for hardware implementation. GDI logic style has emerged as a new logic design style in which the transistor count decreases drastically [9]. By using this method the basic logic functions can be designed using only two transistors which require four, six or even twelve transistor in conventional CMOS logic style [10].

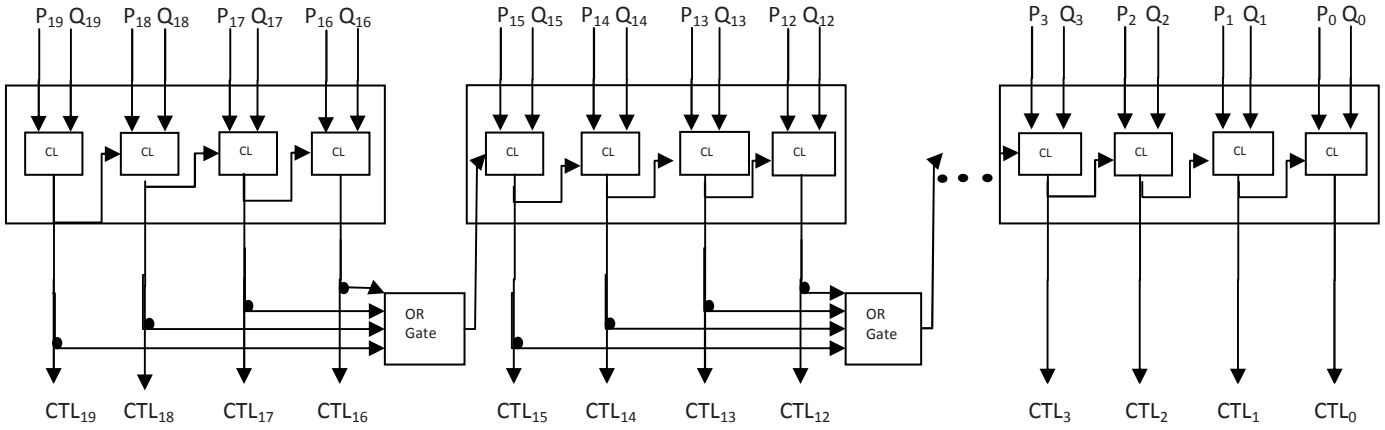

Fig.2. Control Block Structure

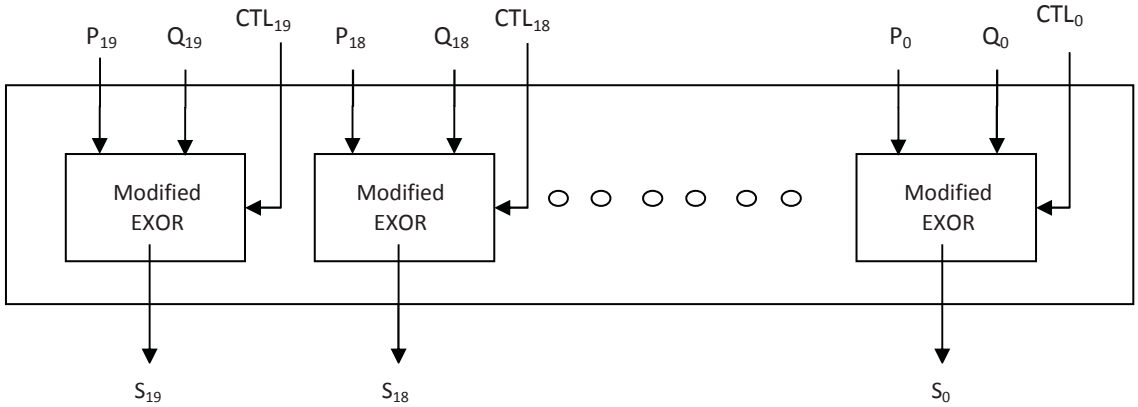

Fig.3. Carry Free Addition Block

A simple GDI cell [11] is shown in figure 4. It is a three input cell where the three inputs are: G (common gate input to both PMOS and NMOS), P (input to source/drain of PMOS) and N (input to source/drain of NMOS).

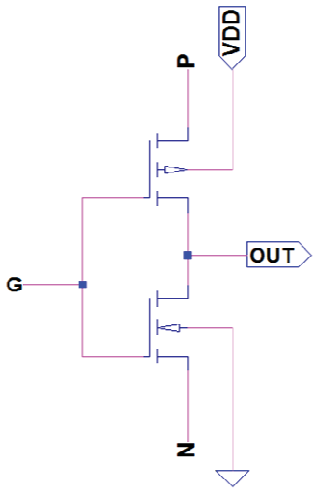

Fig.4. A Simple GDI Cell

Different input combinations are applied to these input pins to obtain various logic functions with lesser number of transistors. Table I shows that a number of Boolean function can be implemented by some simple changes in input configuration using the GDI cell of Fig.4.

Table I: Various Logic Functions Implementation Using GDI Method

N	P	G	Output	Boolean Function
'0'	Y	X	$\bar{X}Y$	F1
Y	'1'	X	$\bar{X}+Y$	F2
'1'	Y	X	X+Y	OR
Y	'0'	X	XY	AND
Z	Y	X	$\bar{X}Y+XZ$	MUX
'0'	'1'	X	$\bar{X}$	NOT

B. *Power Reduction in GDI Technique*

Besides reducing the transistor count, GDI method also improves the power performance of circuit. The sub-threshold leakage current of an NMOS can be given as:

$$I_{SUB} = \frac{W}{L} K' \left(1 - e^{\frac{-V_{ds}}{V_T}}\right) \left(e^{\frac{V_{gs}-V_{th}}{mV_T}}\right)$$

where W is the transistor's width, L is the transistor's length, V_T is the thermal voltage, V_{ds} is the drain-source voltage, V_{gS} is the gate-source voltage, K' and m are process constants, and V_{th} is the threshold voltage.

It can be noticed here that in CMOS logic circuits the pull-up and pull-down networks are always connected to V_{DD} and ground respectively which is not in the case of GDI cell. So a sub-threshold leakage current is always present in CMOS logic circuits whereas in GDI cell, it is absent in almost half of the possible cases. Hence a substantial reduction in power is achieved in GDI cell based designs.

C. *Proposed Architecture*

In our proposed architecture, the accurate and inaccurate parts of ETA are implemented using the GDI cell of Fig.4. In proposed accurate part, the adder cells are designed using GDI logic style [12]. Fig.5 shows the existing and proposed architecture of the adder cells for accurate part. A single adder cell requires 28 transistors when implemented using CMOS logic style whereas it requires only 12 transistors when implemented using GDI technique. It is worth to note here that the delay in ETA is only due the carry propagation in accurate part because no carry propagation occurs in inaccurate part. So as the transistor count is decreased in accurate part, it will improve the overall delay of ETA.

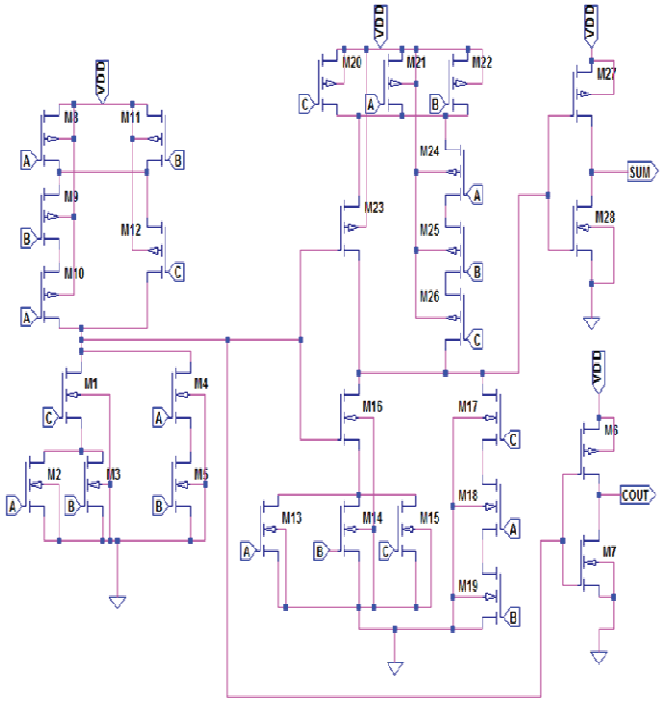

Fig.5(a). Schematic Diagram of Adder Cell Using CMOS Logic Style

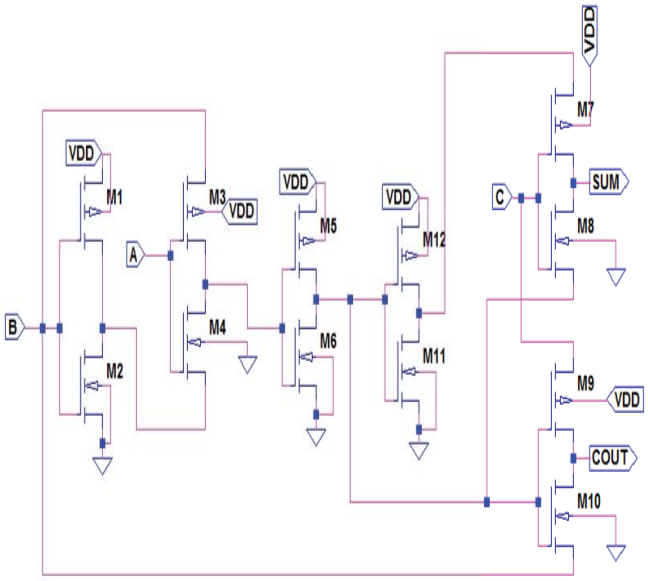

Fig.5(b). Schematic Diagram of Adder Cell Using GDI Logic Style

In similar manner, the MXOR cell in carry free addition block is also implemented using GDI method for our proposed architecture. Fig.6 shows the existing and proposed architecture of MXOR cell. It is clear from the schematic diagram that transistor count is drastically reduced in both adder cell and MXOR cell.

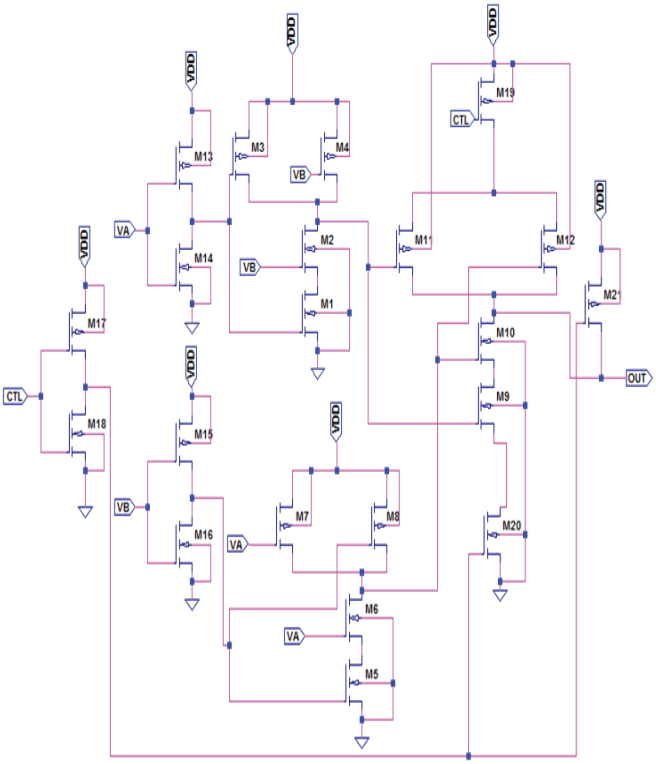

Fig.6(a) Schematic Diagram of MXOR Cell Using CMOS Logic Style

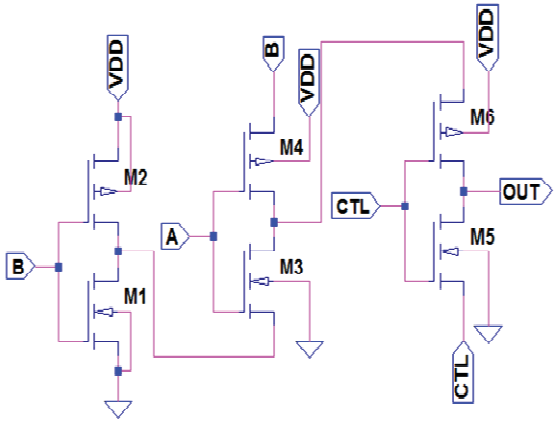

Fig.6(b) Schematic Diagram of MXOR Cell Using GDI Logic Style

IV. RESULTS AND COMPARISON

To illustrate the merits of our proposed GDI based ETA, we simulated it along with the exiting CMOS logic based ETA. Both adders are implemented in 32nm technology. The schematics are drawn in LTspice software. To construct the models of both architectures, HSPICE software is used. 20 sets of input operands are created randomly. Each input set is simulated for both adders and power consumption is recorded. With 20 sets of results, average power was computed. The worst case input was applied to simulate the worst case delay. The worst case input refers to the case when all the input bits of both operands are high. In this case carry will ripple through all the adder cells of accurate part hence resulting in worst case delay. Transistor count was directly obtained from the HSPICE software. A comparative analysis of both designs is shown in Table II.

Table II: Comparative Analysis of ETA Designs

Parameters	Conventional ETA	GDI Based ETA
Transistor Count (N)	1036	544
Delay(ns)	0.50	0.39
Power (μW)	4.36	3.51
PDP (pJ)	2.21	1.38

Simulation results shows that proposed architecture requires 48% less transistor count and attains 38% improvement in power-delay product (PDP). This reduction

in transistor count in our proposed architecture is justified in Table III.

Table III: Justification of Reduced Transistor Count

Part of ETA	Block Name	No. of Cells	Transistor Count in Each Block		Total	
			CMOS Based	GDI Based	CMOS Based	GDI Based
Accurate Part	Adder Cell	12	28	12	336	144
Inaccurate Part	CL	20	12	12	240	240
	OR-Gate	4	10	10	40	40
	MXOR	20	21	6	420	120
Overall Transistor Count					1036	544

V. CONCLUSION

In this paper, a new architecture of ETA is proposed based on GDI logic style. This proposed architecture is implemented and compared with the existing conventional ETA. This new design has outperformed the previous one in terms of power dissipation, speed and transistor count. However, there is a problem of reduced voltage swing in this new design. So to improve the voltage swing, further work can be done in this direction. This proposed architecture can be used in the application where speed, area and power are of greater concern than accuracy.

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