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A Novel Analysis of Sequential Circuits Design Using Reversible Logic

Abstract- *Reversible logic design attracts more interest due to its low power consumption. A lot of research has been done in combinational as well as sequential design of reversible circuits. As far as it is known, this is the first attempt to apply reversible logic to synchronous counters design using T flip-flop. In this paper we have also proposed a new reversible gate which can be used as copying gate. We have proposed a reversible T-Flip-flop which is better than the existing designs by reducing number of gates, garbage outputs and power dissipation. We hope this paper will initiate a new area of research in the field of complex reversible sequential circuits for quantum computers.*

*Keywords —**Low-power** VLSI, Low-power CMOS design, reversible logic, quantum computing, reversible counters.*

I. INTRODUCTION

Reduction of power dissipation remains one of the major goals in the VLSI circuit design for many years. R.Landauer demonstrated in the early 1960s, irreversible hardware computation results in energy dissipation due to the information loss, regardless of its realization technique [1]. It is proved that the loss of each one bit of information dissipates at least KTln2 joules of energy (heat), where K=1.380650 x 10-23 m2kg-2K-1 (joules Kelvin-1) is the Boltzman's constant and T is the absolute temperature at which operation is performed [1]. Reversible logic circuits have theoretically zero internal power dissipation since they do not lose information. Bennett showed that in order to avoid KTln2 joules of energy dissipation in a circuit, it must be built using reversible logic gates [2]. The applications of reversible logic are quantum computation, optical computing, ultra-low power CMOS design [3] and nano- technology. Even though some significant works ([4] - [10]) have been already done in the field of reversible sequential logic design, research on reversible counters has not been done. This paper proposes a novel concept on reversible sequential circuit design which includes asynchronous and synchronous counters. Rest of the paper is organized as follows. Section II provides the idea of basic and necessary reversible logic gates used in this work. Section III provides the details about the proposed reversible gate. Section IV provides the optimized reversible T Flip-flop and its comparison with the existing work. Section V provides the conventional synchronous structure and its reversible design. Section VI concludes the work.

II. REVERSIBLE LOGIC GATES

This section describes the reversible logic gates that are being used in the design. Fig. 1 shows a Feynman Gate. Feynman Gate (FG) can be used as a copying gate. Since a fan-out is not allowed in reversible logic, this gate is useful for duplication of the required outputs.

Fig. 2 shows Sayem Gate [9]. A single Sayem Gate (SG) can be used to realize the function of D-Latch.

Fig. 3 shows the Fredkin Gate (FRG) [11]. This is the most widely used reversible gate.

Fig. 4 shows a Peres Gate (PG). It is also known as New Toffoli Gate (NTG). Functionally Peres Gate is equal with the transformation produced by a Toffoli Gate followed by Feynman Gate.

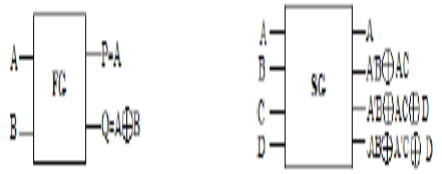

Fig. 1 Feynman Gate Fig. 2 Sayem Gate

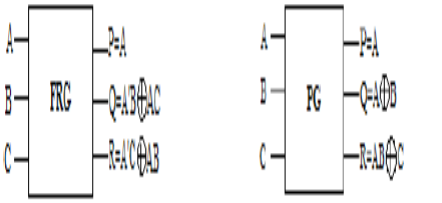

Fig. 3 Fredkin Gate Fig. 4 Peres Gate

III. PROPOSED REVERSIBLE GATE

We have proposed a new conservative reversible gate named RSJ Gate. This is a 2 through 4x4 reversible gates. The block diagram of the proposed gate is shown in Fig. 5. Its corresponding Truth Table is shown in Table I. From this truth table we can verify that the input and output vectors are unique which satisfies the condition of reversibility.

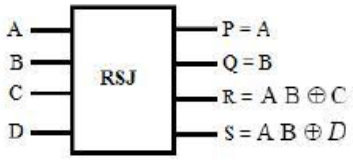

Fig. 5 Proposed RSJ Gate

TABLE I TRUTH TABLE OF THE PROPOSED REVERSIBLE GATE

A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	1
0	1	0	0	0	1	0	0
0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	0
0	1	1	1	0	1	1	1
1	0	0	0	1	0	0	0
1	0	0	1	1	0	0	1
1	0	1	0	1	0	1	0
1	0	1	1	1	0	1	1
1	1	0	0	1	1	1	1
1	1	0	1	1	1	1	0
1	1	1	0	1	1	0	1
1	1	1	1	1	1	0	0

IV. PROPOSED REVERSIBLE POSITIVE EDGE TRIGGERED T FLIP-FLOP

A flip-flop is a bi-stable electronic circuit that has two stable states and can be used as a one-bit memory device. In this section we propose the construction of a Master-Slave T Flip-flop using reversible gates. The truth table of the T Flip-flop is given in Table II. The reversible design is shown in Fig. 6 and the corresponding block diagram is shown in Fig. 7. The reversible realization of T Flip-flop has two SG gates and one Feynman Gate. And it has two constant inputs and it produces three garbage outputs. The comparison of the proposed design with the existing designs is given in Table III. TABLE II POSITIVE EDGE TRIGGERED T FLIP-FLOP

CLK	T	Q_{t-1}	Q
0	0	0	0
1	0	0	0
0	0	1	1
1	0	1	1
0	1	0	0
1	1	0	1
0	1	1	1
1	1	1	0

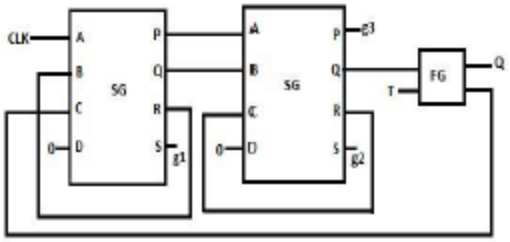

Fig. 6 Reversible Positive Edge Triggered T Flip-flop

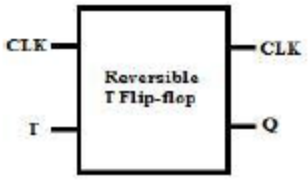

Fig. 7 Block Diagram

TABLE III COMPARISON OF DIFFERENT T FLIP-FLOPS WITH ONLY Q OUTPUT

	No. of Gates	Garbage Outputs	Constant Inputs
Existing [6]	10	12	10
Existing [10]	5	3	2
Existing [5]	10	10	10
Proposed design	3	3	2
Improvement factor w.r.t [6]	3.3	4	5
Improvement factor w.r.t [10]	1.6	-	-
Improvement factor w.r.t [5]	3.3	3.3	5

V. DESIGN OF REVERSIBLE SYNCHRONOUS COUNTER

In the synchronous counters, the count pulses are applied directly to the control/CLK inputs of all the Flip-flops. Synchronous counters have regular pattern and can be constructed using flip-flops and gates.

A. Proposed 4-bit Synchronous Down-Counter

A conventional 4-bit Synchronous down Counter with count enable function can be realized as shown in Fig.8. The reversible design of the above 4-bit Synchronous down Counter is shown in Fig. 9. The proposed RSJ gates are used to produce the copy of the Q output of the T Flip-flops. The Peres gate is used to realize the AND function. The proposed reversible synchronous counter design contains 15 reversible gates, 13 constant inputs and produces 12 garbage outputs.

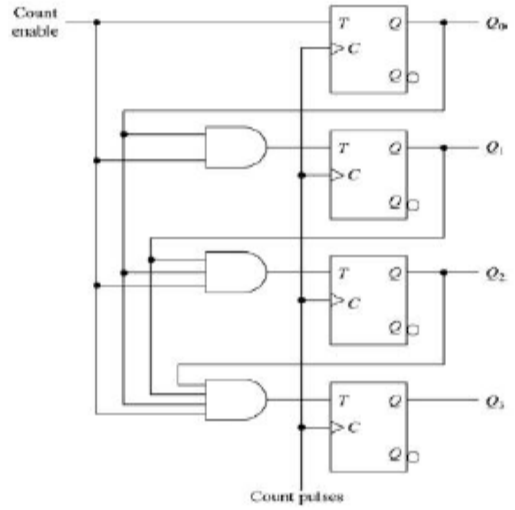

Fig. 8 Conventional 4-bit Synchronous Down-Counter

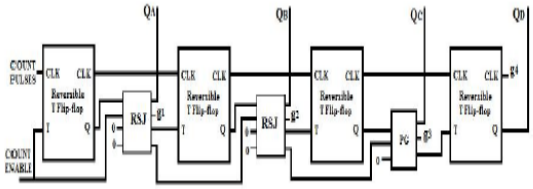

Fig. 9 Proposed 4-bit reversible synchronous down counter

B. Proposed 4-bit Synchronous Up/Down Counter

The conventional 4-bit Synchronous Up/Down-Counter is shown in Fig.10. The reversible design of this 4-bit Synchronous Up/Down Counter is shown in Fig. 11. The proposed RSJ gates are used to produce the copy of the Q output of the T Flip-flops. The Peres gate is used to realize the AND function. The proposed reversible synchronous counter design contains 18 reversible gates, 18 constant inputs and produces 16 garbage outputs.

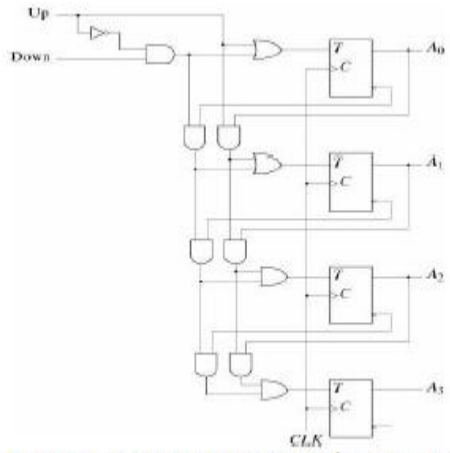

Fig. 10 Conventional 4-bit Synchronous Up/Down Counter

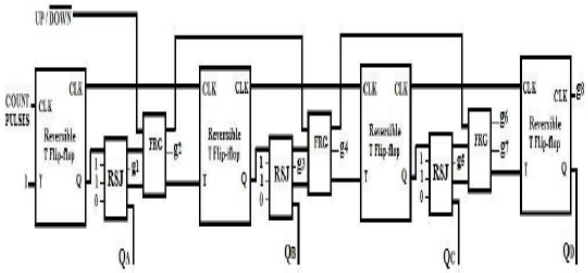

Fig. 11 Proposed 4-bit reversible synchronous Up/Down Counter

VI. CONCLUSIONS

The key contribution of this paper is the reversible realization of 4-bit synchronous counters by using proposed reversible gates and the existing one. As far as it is known, this is the first attempt to apply reversible logic to synchronous counter design. We also have proposed a new conservative reversible gate. This gate can be used to produce multiple copies of a signal. The proposed synchronous counter designs have the applications in building reversible ALU, reversible processor etc. This work forms an important move in building large and complex reversible sequential circuits for quantum computers. The future work could be to develop efficient reversible counters and reversible controller circuits.

ACKNOWLEDGMENT

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