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The design of high performance Barrel Integer Adder

Abstract: This paper proposes a new kind of parallel integer addition algorithm - the barrel integer addition algorithm on the basis of researching the structure of half adder. It also elaborates the principle and structure of barrel integer addition algorithm, analyses the time and the degree of complexity in the area of the algorithm and at the same time compares it with the traditional integer addition algorithm. We realized that the 16-bit barrel integer adder using Verilog HDL and verifies comprehensively in the Altera device. The result shows that the speed of the barrel integer adder designed in this paper improves obviously on the basis of a small increase of area, which lays the foundation for the improvement of the multiplier performance.

Key words: half adder; barrel integer adder; FPGA; algorithm

I.INTRODUCTION

Arithmetic Logic Unit (ALU), a very important part of microprocessor chip, can not only complete the arithmetic operation but also the logic operation [1]. However, all the basic arithmetic operations (subtraction, multiplication, division) can eventually be reduced to the addition operation, so the realization of the addition operation is particularly important. In order to reduce the time of binary transmission and improve the speed of computing, people have designed various types of adders and raised a lot of methods to achieve adders, such as ripple carry adders, fast ripple carry adders, super-head carry adders, etc. The adders mentioned above are all ofthe parallel ones. In addition, there is also a kind of serial adder, which on the one hand has the advantages of less resources and flexible designs, etc; on the other hand, affects the speed of serial carry adder because of the gradual carry.

2. METHODOLOGY

2.1 HA (Half Adder):

The adder is a kind of basic arithmetic operation of digital circuits and digital systems, while subtraction, multiplication and division are all realized based on addition. In digital systems, the addition operation is achieved through logic operation. The adder which does not contain binary within addition is called half-adder; otherwise known as the full-adder. The Half Adder (HA) is a kind of logic circuit which considers A and B as inputs to produce an output S and an output carry *Cout* [2], the logic relation is shown as follows:

$$\begin{cases} S = A \oplus B \\ C_{out} = A \cdot B' \end{cases} \quad (1\text{-}1)$$

The logic circuit is shown as in Figure 1, which is made up of an AND gate and an exclusive OR gate.

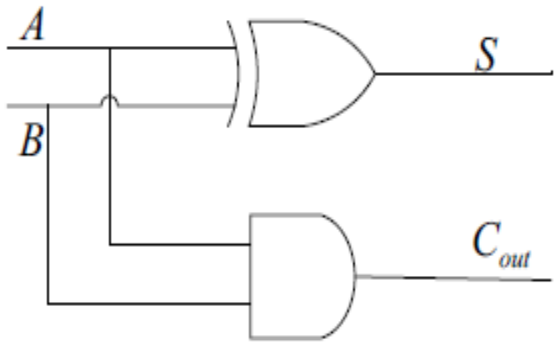

Figure 1.the logic circuit of half-adder

The half-adder (HA) corresponding to Figure 1may also be shown by which tells the relationship between input and output (Figure 2).

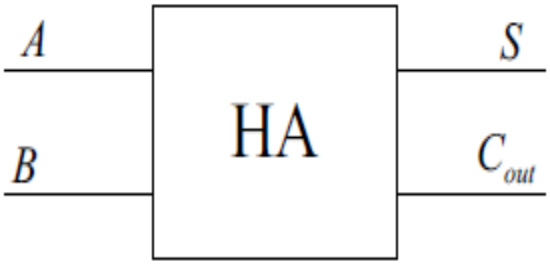

Figure 2. The Schematic Diagram of half-adder

2.2 The Principle of Barrel Integer Addition Algorithm

Barrel Integer Addition Algorithm is a kind of parallel one based on the half-adder, of which basic principles are as follows:

Suppose addend A and summand B are two binary numbers with n bits, using superscripts for time variables and subscripts for binary bits, while *Ak* ,*Bk* are considered as the completion of the *k* meeting of iteration by A and B, that is:

$$A^k = A_{n+1}^k A_n^k A_{n-1}^k \cdots A_i^k \cdots A_3^k A_2^k A_1^k, \quad (2\text{-}1)$$

$$B^k = B_{n+1}^k B_n^k B_{n-1}^k \cdots B_i^k \cdots B_3^k B_2^k B_1^k, \quad (2\text{-}2)$$

k=0,1,2…….

The highest A_{n+1}^k 、 B_{n+1}^k are the carry bits added to the carries, there are $A_{n+1}^0 \equiv 0$, $B_{n+1}^0 \equiv 0$. Obviously:

$$A = A^0 = A_{n+1}^0 A_n^0 A_{n-1}^0 \cdots A_i^0 \cdots A_3^0 A_2^0 A_1^0,$$

$$B = B^0 = B_{n+1}^0 B_n^0 B_{n-1}^0 \cdots B_i^0 \cdots B_3^0 B_2^0 B_1^0 \quad (2\text{-}3)$$

are the initial number of iteration. The iterative formula of half-adder is defined as:

$$S_i^k = A_i^{k-1} \oplus B_i^{k-1}, \quad (2\text{-}4)$$

$$C_i^k = A_i^{k-1} \cdot B_i^{k-1}, \quad (2\text{-}5)$$

$i = 1,2,3,\cdots,n+1; \quad k = 1,2,\cdots.$

The equation (2-4) is the addition, while equation (2-5) is the carry; order

$$A_i^k = S_i^k, \quad (2\text{-}6)$$

$$B_1^k = C_{n+1}^k, B_i^k = C_{i-1}^k, \quad (2\text{-}7)$$

i=1,2,3……n;k=1,2,3……

a new set of summands and additions can be obtained.

$$A^k = A_{n+1}^k A_n^k A_{n-1}^k \cdots A_i^k \cdots A_3^k A_2^k A_1^k, \quad (2\text{-}8)$$

$$B^k = B_{n+1}^k B_n^k B_{n-1}^k \cdots B_i^k \cdots B_3^k B_2^k B_1^k, \quad (2\text{-}9)$$

$k = 1,2,\cdots.$

It can prove that C_k=0, then

$$A + B = A^k = S. \quad (2\text{-}10)$$

The structure of Barrel Integer Adder is shown in Figure 3, where HA represents the half-adder, D the flip-flop, *i C* the control terminal of flip-flop. The Barrel adder is referred to CBA (Carry Barrel Adder) for short.

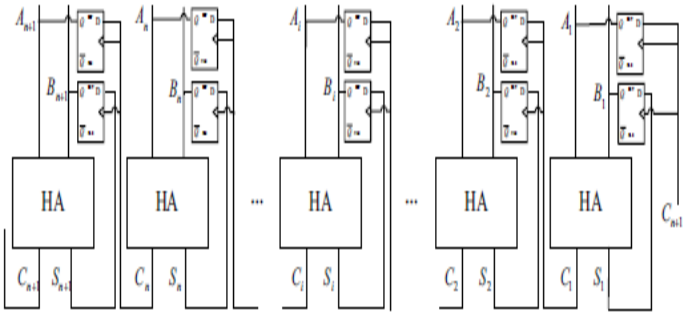

Figure 3.The structure of Barrel Integer Adder

2.3 Complexity Analysis

Barrel Integer Addition Algorithm is a kind of integer addition algorithm with the combination of parallel and iteration. The average times of iterations directly determine the performance of the algorithm, and the definition of the average times of iterations is just like the equation (2-11) as follows:

The average times of iterations = total times of iterations/total times of additions (2-11)

Binary numbers have only two kinds of forms 0 and 1. The binary numbers of N-bit have altogether 2_N kinds of combinations, and the total times of additions is $2^N \times 2^N$ the total times of iterations are the summation of iteration times of N-bit binary numbers. Take N=2for example, consider the summand and addend respectively As A=11,B=01, the iterative process is shown in Figure 4.

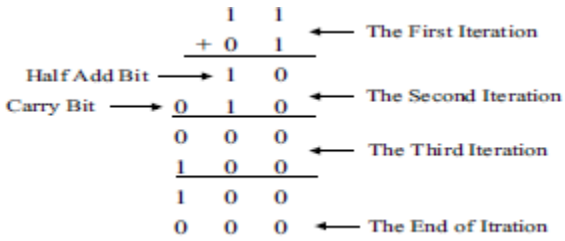

Figure 4. Schematic diagram of the iterative process of A+B

Accordingly, the times of iterations of all the combinations when N is defined as 2, as shown in Table 1. According to Table 2, where the average number of iterations of the N=1, 2 …8, the average times of iterations of the barrel integer addition algorithm can be calculated $O(\log_2 (n+1))$,approximately. At the same time, according to the structure of the CBA in Figure 3, we can see that there should only be N+1half-adder for the addition of two N-bit binary numbers. Therefore, the time and area complexity of a barrel integer adder are $O(\log_2 (n+1))$, $O(n+1)$ respectively.

Table1. Times of iterations when N=2

	00	01	10	11
00	0	0	0	0
01	0	2	1	3
10	0	1	2	2
11	0	3	2	2

Table 2. The average times of iterations when N-1, 2…8

Decimals	total times of additions	total times of iterations	the average times of iterations
1	4	2	0.500
2	16	18	1.125
3	64	106	1.656
4	256	532	2.078
5	1024	2478	2.419
6	4096	11072	2.703
7	16384	48246	2.944
8	65536	206736	3.155

Table 3. The comparison of different types of adders in time and area of complexity.

Types of adders	Time complexity	area complexity
CRA	$O(n)$	$O(n)$
SCA[4]	$O(\sqrt{n})$	$O(n)$
CSA[5]	$O(\sqrt{n})$	$O(n)$
CLA[6]	$O(\log_2 n)$	$O(n\log_2 n)$
CBA	$O(\log_2(n+1))$	$O(n+1)$

Table3 is the comparison of different types of integer adders in time and area complexity .In the aspect of time complexity, the barrel integer adder is similar to the best super-head carry adder [3]; in the aspect of the area complexity, the barrel integer adder is better than the super-head binary adder and similar to other integer adders. Therefore, from the integrated perspective of time and area, the complexity of barrel integer adder is better than several other commonly used integer adders, while barrel integer adder is based on the half-adder, with simple and regulated structure, short-delayed path and convenient extension circuit.

3. DESIGN CONSTUCTION AND SIMULATION

3.1 FPGA Realization of the Barrel Integer Adder

The role of each port signal of barrel integer adder is shown as in Table 4. The barrel integer adder is achieved by the state machine approach [7], the transition of state is shown in Figure5, composing of four states: idle, half adder, judge and over. The conditions of conversions among different states have been marked.

Table 4.Barrel integer adder signal definition table

Signal	Effect
clk	Barrel addition algorithm clock select signal
rst	Reset signal
A	Summand input signal
B	Addend input signal
S	Output addition signal

3.2 Simulation results

To take the design of 16-bit barrel integer adder for example, the compiled Verilog code have all been compiled, and table 5 is the inclusive compiled result of CBA, of which the maximum clock frequency reaches to 230.21 MHz. When using SignalTapII added to QUARTUS software to simulate, the timing simulation result is shown in Figure 6.A for 1111111000111010b, B for 1111110000111111b, S for 1111110100111100 1b (1FA79h), the simulation result is correct.

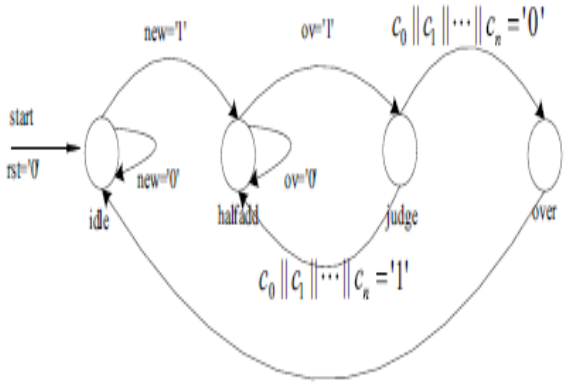

Figure 5. The state transition diagram for Barrel integer addition algorithm

Table 5 the module compiled results of 16-bit adder

Items	Occupied logic elements (LE) / resources utilization	Maximum Clock Frequency	The worst delay	Worst-case tsu	Worst-case tco	Worst-case th
Results	93 / (<1%)	230.21 MHz	2.612 ns	-0.344ns	10.388 ns	2.099 ns

4. CONCLUSION

Table 6, Table 7, Figure 7 are about the performance comparisons conducted in the total same compiled and comprehensive conditions of five kinds of 16-bit integer adders, in which resources utilization = speed/ LE Occupancy, we can analyze and see:

1) As For the barrel integer adders with the same carry, the speed has greatly increased, and improved obviously on resources utilization in spite of some rise in resource occupancy.

2)The barrel integer adder designed in this chapter effectively has improved the speed of integer addition algorithm , and the speed of 106 bits barrel integer adder reached 151.03 MHZ, which has laid a good foundation for the design of double-precision floating-point multiplier.

3) The volume of decreasing speed of the barrel integer adders is reduced greatly with the increases of the bits, so it has obvious advantages in the addition of the high level.

Table 6 16 the comparison of 16-bit in FPGA realization

Types of adders	LE occupancy	speed (MHZ)	resource utilization (E)
CLA	72	53.27	0.740
SCA	58	42.99	0.741
RCA	32	29.35	0.917
CSA	63	45.32	0.758
CBA	93	230.12	2.474

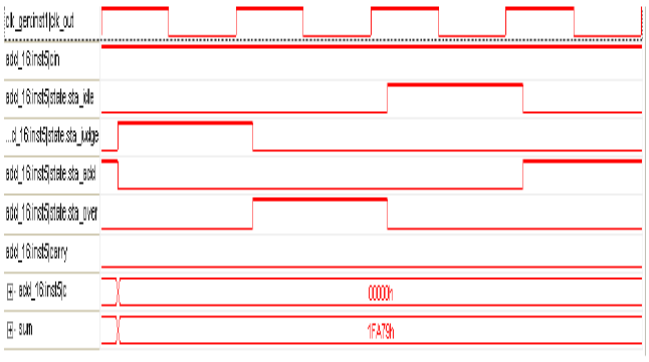

Figure 6 Timing Simulation of 16-bit adder

Table7 The simulation result of different bits for CBA

Adder bits(bit)	Occupied logic element	The highest clock frequency
4	28	372.44
8	51	355.37
16	93	230.12
32	178	192.20
64	352	152.28
106	560	151.03
128	582	149.37

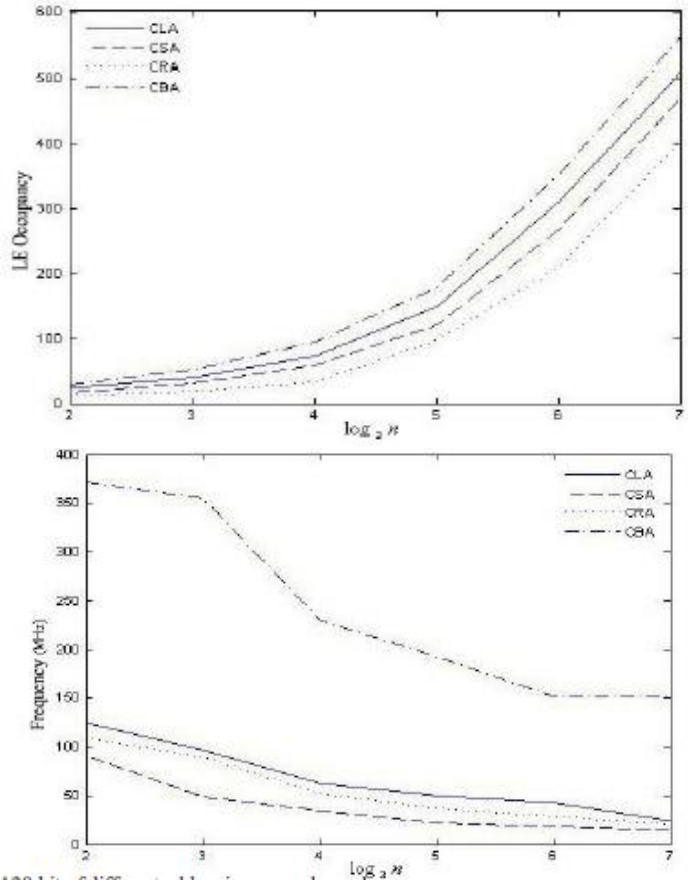

Figure 7 the comparisons of 4,8,16,32,64,128-bit of different adders in area and speed

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