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Modified TOFFOLI GATE and its Applications in Designing Components of Reversible Arithmetic and Logic Unit

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ABSTRACT - Reversible logic has received great attention in the recent years due to it's ability to reduce the power dissipation which is the main requirement in low power digital design. It has wide applications in advanced computing, low power CMOS design, Optical information processing, DNA computing, bio information, quantum computation and nanotechnology. This paper presents a modified Toffoli gate(MTG) and its applications in designing components of a Reversible Arithmetic and Logic unit. The quantum cost and quantum realization of MTG is proposed in this work. All the components have been modeled and functionally verified using VHDL and ModelSim.

Keywords-Advanced computing, Modified Toffoli gate, Reversible arithmetic unit, Reversible logic circuits.

I. INTRODUCTION

Conventional combinational logic circuits dissipate heat for every bit of information that is lost during their operation. Due to this fact the information once lost cannot be recovered in any way. But the same circuit, if it is constructed using the reversible logic gates will allow the recovery of the information. In 1960s R. Landauer demonstrated that even with high technology circuits and systems constructed using irreversible hardware, results in energy dissipation due to information loss [1].He showed that the loss of one bit of information dissipates KTln2 joules of energy where K is the Boltzman's constant and T is the absolute temperature at which the operation is performed [1]. Later Bennett, in 1973, showed that this KTln2 joules of energy dissipation in a circuit can be avoided if it is constructed using reversible logic circuits [2].

A reversible logic gate is an n-input, n-output logic device with one-to-one mapping. This helps to determine the outputs from the inputs but also the inputs can be uniquely recovered from the outputs. Additional inputs or outputs are added so that the number of inputs are made equal to the number of outputs whenever it is necessary. An important constraint present on the design of a reversible logic circuit using reversible logic gate is that fan-out is not allowed. A reversible circuit should be designed using minimum number of reversible gates. One key requirement to achieve optimization is that the designed circuit must produce minimum number of garbage outputs, also they must use minimum number of constant inputs [3, 4].

The Present paper proposes quantum realization of MTG which is used to design the components of a reversible Arithmetic and Logic unit. The proposed work is found to be an optimized design.

II. NEED FOR REVERSIBLE LOGIC GATES

A. Reversible logic

The reversible logic operations do not erase (lose) information and dissipate very less heat. Thus, reversible logic is likely to be in demand in high speed power aware circuits. Reversible circuits are of high interest in low-power CMOS design , optical computing, quantum computing and nanotechnology. The most prominent application of reversible logic lies in quantum computers. A quantum computer can be viewed as a quantum network composed of quantum logic gates or circuits; each gate performs an elementary unitary operation on one, two or more two–state quantum systems called qubits. Each qubit represents an elementary unit of information corresponding to the classical bit values 0 and 1. The quantum networks cannot be directly deduced from their classical Boolean counterparts which are clearly irreversible. Thus, quantum arithmetic must be built from reversible logic components [12]. The reversible logic gate or circuit is a n-input n-output logic function in which there is a one-to-one correspondence between the inputs and the outputs. Because of this bijective mapping the input vector can be uniquely determined from the output vector. This prevents the loss of information which is the root cause of power dissipation in irreversible logic circuits.

From the point of view of reversible circuit design, there are many parameters for determining the complexity and performance of circuits [3, 4 and 8].They are listed below.

The number of Reversible gates (N): The number of reversible gates used in circuit.

The number of constant inputs (CI): This refers to the number of inputs that are to be maintained either at 0 or 1 in order to synthesize the given logical function.
The number of garbage outputs (GO): This refers to the number of unused outputs present in a reversible logic circuit. One cannot avoid the garbage outputs as these are very essential to achieve reversibility.
Quantum cost (QC): This refers to the cost of the circuit in terms of the cost of a primitive gate. It is calculated knowing the number of primitive reversible logic gates (1*1 or 2*2) required to realize the circuit.

B. Important reversible logic gates

Feynman gate [5, 6], and BVF gate [11] are the two reversible logic gates used in this work , along with the MTG.

1) *Feynman / CNOT Gate (FG):* Fig 1. shows the Feynman gate which is a 2*2 gate and is also called as Controlled NOT and it is widely used for fan-out purposes. The inputs (A, B) and outputs P=A, Q= A⊕B. It's Quantum cost is one.

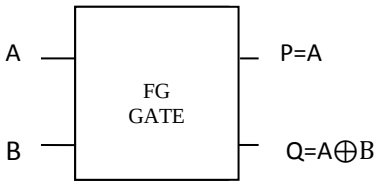


Fig.1a. Feynman Gate – 2*2 gate

2) BVF Gate: The Fig 2 shows a 4*4 gate with inputs (A,B,C,D) and ouputs (P=A, Q= A⊕B, R=C, S= C⊕D). It's quantum cost is two.

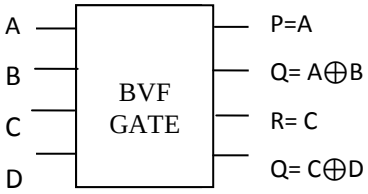
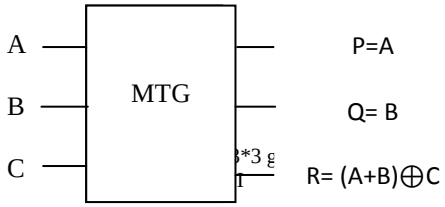


Fig.2. BVF gate – 4*4 gate

III. Proposed Quantum realization of MTG (Modified Toffoli Gate)

The authors in [13] have proposed MTG as a 3 inputs 3 outputs gate having inputs to outputs mapping as P=A, Q=B and R =(A+B) ⊕ C. The proposed quantum realization of this gate is shown in fig 3.1. The MTG is designed from two controlled V gate and two CNOT gate resulting in quantum cost of 5. Further logic depth of quantum implementation of MTG is 5. This results in propagation delay as 5 Δ , where Δ is the unit delay. Table 1 shows the truth table of MTG.



TRUTH TABLE OF MTG

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	1
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	1	0	0
1	1	0	1	1	1
1	1	1	1	1	0

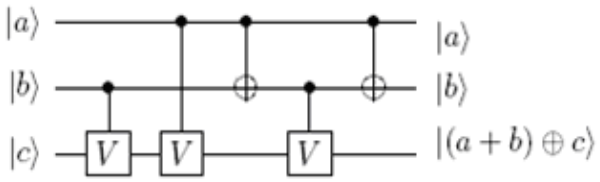


Fig 3.1. Quantum realization of MTG

A. Application of MTG

MTG can be used for the following applications.

1. Fan-out
2. Logical operations
3. Arithmetic operations

1) MTG can be used for fan-out purpose by applying constant inputs at it's inputs which is summarized as shown in the table.2

TABLE II
MTG AS A FAN-OUT GATE

A	B	C	P	Q	R
A	0	0	A	0	A
0	B	0	0	B	B

2) MTG can be used as a logical gate by changing the control bits at inputs. The following Table III summarizes the functioning of MTG as universal or logic gate.

Table III
MTG AS UNIVERSAL GATE

A	B	C	P	Q	R	Gate Function
A	B	0	A	B	A+B	OR
A	B	1	A	B	(A+B)'	NOR
0	A	B	0	A	A⊕B	XOR
1	A	B	1	A	A⊕B	XOR
A'	B'	0	A'	B'	(AB)'	NAND
A'	B'	1	A'	B'	AB	AND
A	0	1	A'	B'	A'	NOT

3) MTG can be used to perform addition and subtraction using additional gates. Proposed arrangements to perform various arithmetic operations are as follows.

(i) One's complementer and subtractior using 1's Complement is as shown in fig 3.2

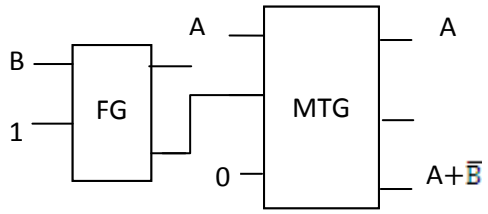


Fig 3.2 one's complementer

(ii) Two's complementer is as shown in Fig 3.3

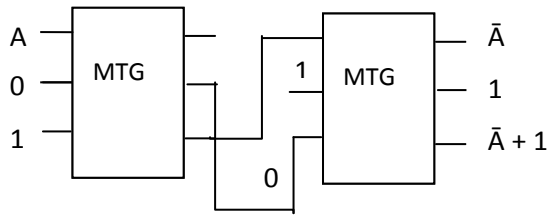


Fig 3.3 Two's complementer

(iii) Half adder using BJN and BVF gate is as shown in Fig 3.4

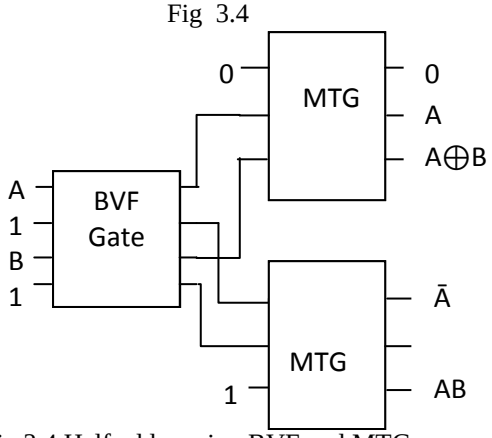


Fig 3.4 Half adder using BVF and MTG

(iv) Half subtractor using MTG and BVF gate is as shown in fig. 3.5.

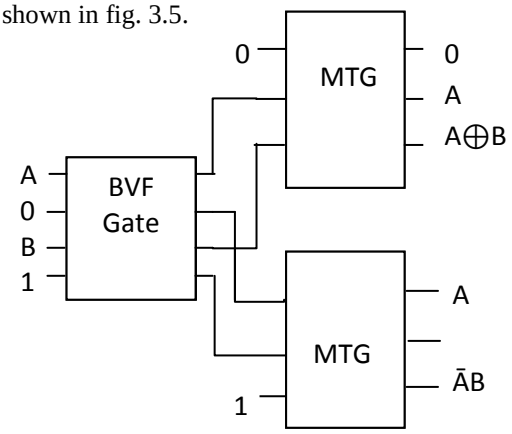


Fig 3.5 Half subtractor using BVF and MTG

(v) One bit Comparator using MTG is shown in Fig 3.6

TABLE IV
TRUTH TABLE OF 1- BIT COMPARATOR

Input		Output		
A	B	$F_{A>B}$	$F_{A=B}$	$F_{A<B}$
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

A one bit comparator can be realized using the proposed MTG. The truth table of one bit comparator is as shown in Table IV.

It is observed from the above table that, if any two conditions are not satisfied, then the third condition will be true. So one of the output can be generated from the remaining two outputs and thus the logic depth of the circuit reduces since computation is carried out with one gate. This novel idea optimizes the design in terms of gate count, garbage output, c[illegible] inputs and quantum cost.

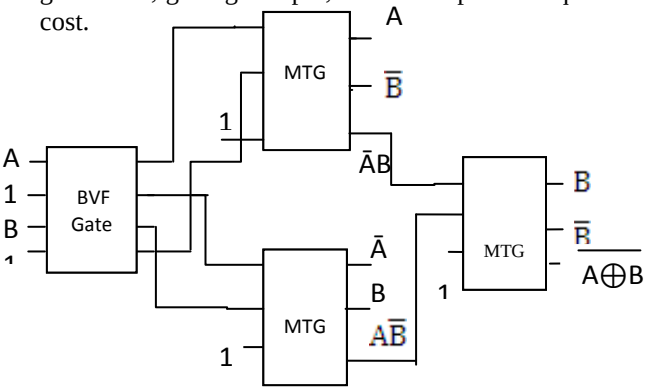


Fig. 3.6 one bit comparator using MTG

(vi) Pattern Detector

Sequence or pattern detector plays an important role in bit error testing method for digital communication circuits. Among the common types of bit error rate test patterns all ones and all zeroes detector are useful in indicating the certain alarm signals.

(vi.a) All One Detector: This type of detectors is used to detect a pattern composed of ones only. An unframed all ones pattern is used to indicate an alarm indication signal. It is shown in Fig 3.7.

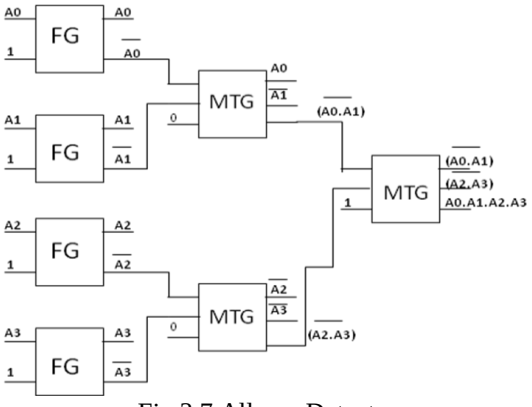


Fig 3.7 All one Detector

(vi.b) All Zero Detector: This type of detectors are used to detect a pattern composed of zeros only. It is effective in finding equipment mis-optioned for alternate mark position such as fiber/radio multiplex low-speed inputs. It is shown in Fig 3.8.

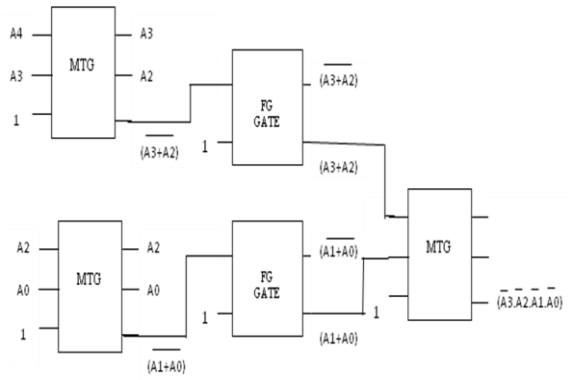


Fig 3.8 All Zero Detector

The Performance parameters such as Quantum cost and delay for all the proposed designs are listed in Table 5.

TABLE V
PERFORMANCE PARAMETERS OF DESIGNS

Sl. No.	Design	Quantum cost	Delay in delta
1	One's complementor	6	6
2	Two's complementor	10	10
3	Half adder	12	7
4	Half subtractor	12	7
5	One bit comparator	17	12
6	All one detector	19	11
7	All zero detector	17	11

IV. CONCLUSION

The focus of this paper is the application of a reversible 3*3 MTG to design the components of a primitive reversible Arithmetic and logic Unit. All the designs lead to a high speed and low power reversible circuits. The proposed structures are analyzed in terms of technology independent implementations. The circuits designed here using MTG can be used for designing large reversible circuits. Thus, this paper provides the initial threshold to build more complex reversible systems. The performance parameters are optimized in comparison with the existing numerical comparators [10].

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