

Realization of 2:4 reversible decoder and its applications

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Abstract— In this paper realization of 2:4 reversible decoder is proposed which can provide active high as well as active low outputs. The proposed decoder uses Feynman and Fredkin gates and has low quantum cost. The proposed gate is first extended to 3:8 decoder followed by an n-input decoder. The theoretical proposition is verified through SPICE simulations. A comparison with existing reversible decoders is also included.

Keywords—Reversible decoder, Feynman and Fredkin gates

I. INTRODUCTION

The encoded input information need be preserved at the output in computational tasks pertaining to digital signal processing, communication, computer graphics, and cryptography applications [1]. The conventional computing circuits are irreversible i.e. the input bits are lost when the output is generated. This information loss during computation culminates into increased power consumption. According to Landauer [2], for each bit of information that is lost during the computation generates $KT \ln 2$ Joules of heat energy where K and T respectively represent Boltzmann's constant and absolute temperature. The information loss becomes more frequent for high speed systems thereby leading to increased heat energy. C. Bennett [3] demonstrated that power dissipation in can be significantly reduced the same operation is done reversibly. Reference [4] describes that reversible logic allows the circuit to go back at any point of time therefore no bit of information is actually lost and the amount of heat generated is negligible.

In digital design, decoders find extensive usage - in addressing a particular location for read/write operation in memory cells [5], in I/O processors for connecting a memory chips to the CPU [6]; and also in Analog to Digital (ADC) and Digital to Analog Converters (DAC) which are used in various different stages of a communication system. This paper therefore addresses the design of reversible decoders. The literature survey on reversible decoders [7 - 11] shows that the focus is on either developing topology based on available reversible gates [7 - 9] or present an altogether new gate for the

said purpose [10, 11]. The topology [7] employs Double Feynman and Fredkin gates for realization whereas the one presented in [8, 9] is based on Fredkin gates. The former topology is cost efficient and later has higher cost metrics. Comparatively larger number of constant inputs and garbage outputs are present in [7]. A new gate R2D is proposed in [10] for developing reversible decoders. It, however, has large constant inputs and garbage outputs. Yet another reversible decoder is presented in [11] which has attractive cost metrics but it cannot be extended further into a generalized n- input decoder. The reversible decoders [7-11] provide only active high mode of operation. This study introduces a reversible decoder which can provide both active high and active low mode of operation and utilizes Feynman and Fredkin gates. A comparison in terms of number of constant inputs, quantum cost and the number of garbage outputs is also given. The proposed topology is implemented using transmission gates. The functionality of the theoretical proposition is verified through SPICE simulations using 180 nm TSMC CMOS technology parameters

II. BACKGROUND AND BASIC CONCEPTS

Reversible gates have equal number of inputs and outputs; and each of these input output combination is unique. An n input n output reversible gate is represented as $n \times n$ gate. The inputs which assume value '0' or '1' during the operation are termed as constant inputs. On the other hand, the number of outputs introduced for maintaining reversibility is called garbage outputs. Some of the most widely and commonly used reversible gates are Feynman Gate (FG), Fredkin Gate (FRG), Peres gate (PG) and Toffoli gate (TG). Out of these gates Feynman gate is a 2×2 gate while Peres, Toffoli and Fredkin gates belong to 3×3 gates. The cost of reversible gate is given in terms of number of primitive reversible gates needed to realize the circuit [12].

The proposed work is based on Feynman and Fredkin gates [13, 14] whose quantum representation is given in Fig. 1. The quantum cost of these gates is one and five respectively.

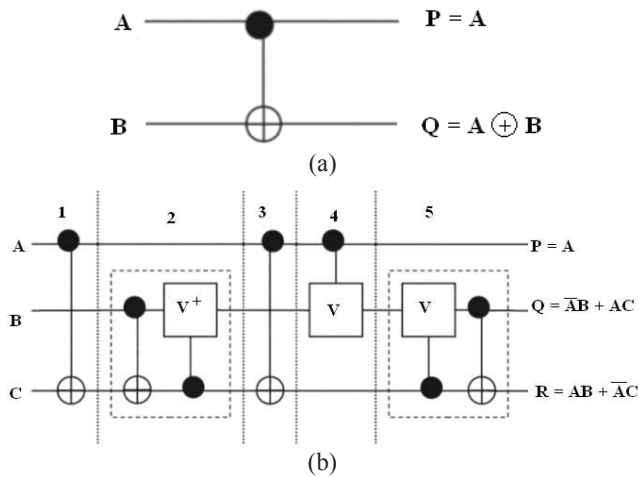


Fig. 1. Quantum representation of (a) Feynman and (b) Fredkin gates [13,14]

A. Proposed 2:4 Reversible Decoder

The proposed 2:4 Reversible decoder is shown in Fig. 2. It uses two Feynman gates (FG) and two Fredkin gates (FRG). It has three inputs A, B and S where A and B are the inputs to the decoder and S is the select line which will select the mode of operation for decoder. The output lines of decoder are taken from the outputs of the two cascaded Fredkin gates wherein each of the Fredkin gates provides two of the four outputs of the decoder. The active high outputs are achieved for S=0, therefore only a single output will be at logic high and all other outputs will be at logic low. Conversely, S=1 provides active low operation thus single output will be at logic low and all other outputs will assume logic high. The operation of the circuit is given in Table 1. The proposed decoder uses two constant inputs and a single garbage output; and has quantum cost of 12. Thus, the proposed circuit performs the operation in active high as well as active low mode in a very cost efficient manner. The next section describes the implementation of 3:8 decoder using decoder of Fig. 2.

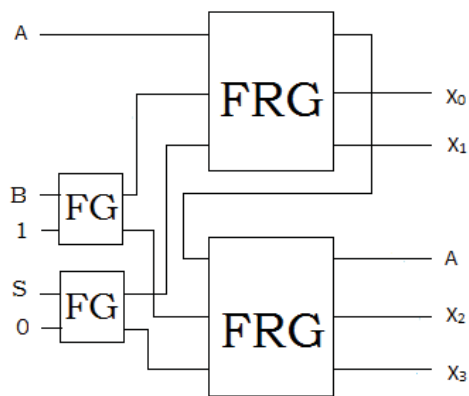


Fig. 2. Proposed 2:4 Reversible Decoder

Table 1 Truth Table for proposed 2:4 reversible decoder

Inputs		Outputs(S = 0)				Outputs(S = 1)			
A	B	X ₂	X ₀	X ₃	X ₁	X ₀	X ₂	X ₁	X ₃
0	0	1	0	0	0	0	1	1	1
0	1	0	1	0	0	1	0	1	1
1	0	0	0	1	0	1	1	0	1
1	1	0	0	0	1	1	1	1	0

B. Proposed 3:8 Reversible Decoder

The block diagram of the proposed 3-to-8 decoder is shown in Fig. 3 where A, B and C are the inputs to the decoder, S is the select line and Y_i (i = 0, 1, ..7) represent the outputs. It uses the proposed 2-to-4 decoder and cascade it with Fredkin and Feynman gates. It also uses an additional 1 to 5 tracer circuit in order to remove the fan out problem in the reversible decoder in case S had been the output of any other reversible gate. This block copies input S to 5 different lines and comprises of Feynman gates. Each of the tracer circuit output is applied to the input to the Fredkin gates. The tracer circuit, however, will not be needed if S is the not an output of any other reversible gate. Table 2 and 3 show the truth tables of the proposed decoder with select line S = 0 and 1 respectively.

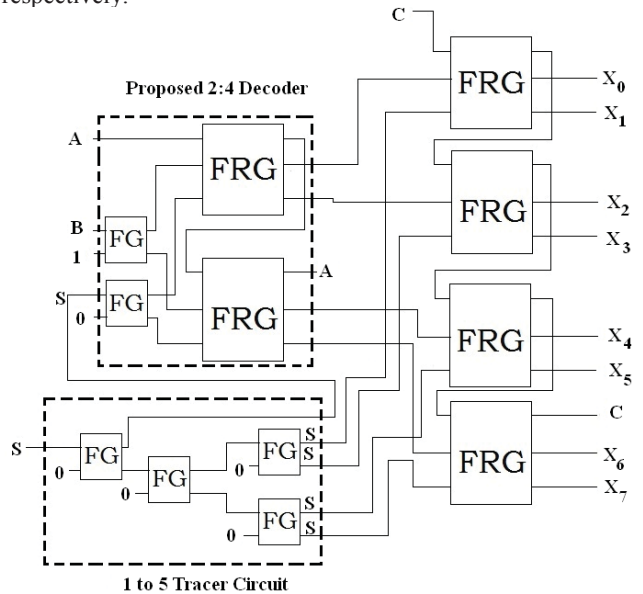


Fig. 3. Proposed 3:8 Reversible Decoder

The proposed 3:8 decoder can easily be extended to a generalized m: 2^m reversible decoder where n is greater than or equal to 3. The generalized decoder will use a 1 to (2^m - 3) tracer circuit which will copy the input S to each of the 2^m - 3 lines and can easily be implemented by using Feynman gates in the same manner in which 1 to 5 tracer circuit was

implemented. Figure 4 shows the generalized $m:2^m$ reversible decoder, here A_1, A_2, \dots, A_m are its inputs and outputs are represented as Z_0, Z_1, \dots, Z_n ($n=2^m$), and S is the select line.

Table 2 Truth table for Proposed 3:8 reversible Decoder with $S=0$

Inputs			Outputs							
A	B	C	Y_4	Y_5	Y_1	Y_0	Y_6	Y_7	Y_2	Y_3
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	0	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	0	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

Table 3 Truth table for Proposed 3-to-8 reversible Decoder with $S=1$

Inputs			Outputs							
A	B	C	Y_0	Y_1	Y_4	Y_5	Y_2	Y_3	Y_6	Y_7
0	0	0	0	1	1	1	1	1	1	1
0	0	1	1	0	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1
0	1	1	1	1	1	0	1	1	1	1
1	0	0	1	1	1	1	0	1	1	1
1	0	1	1	1	1	1	1	0	1	1
1	0	0	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	0

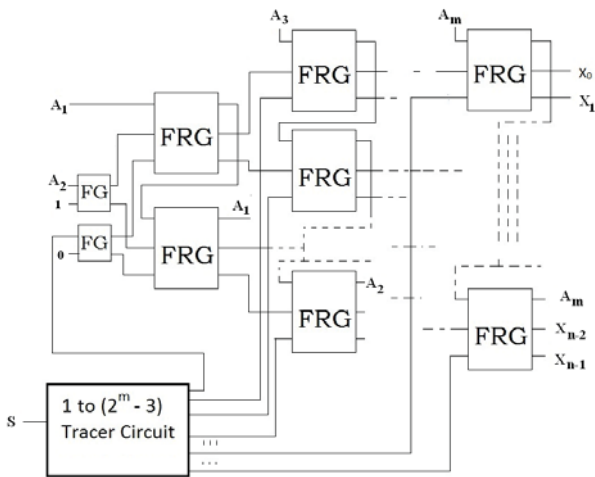
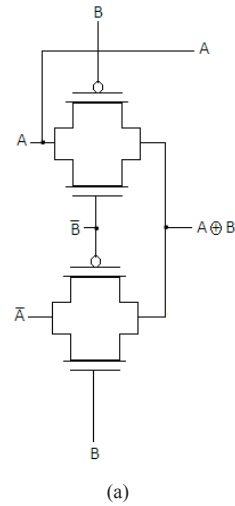


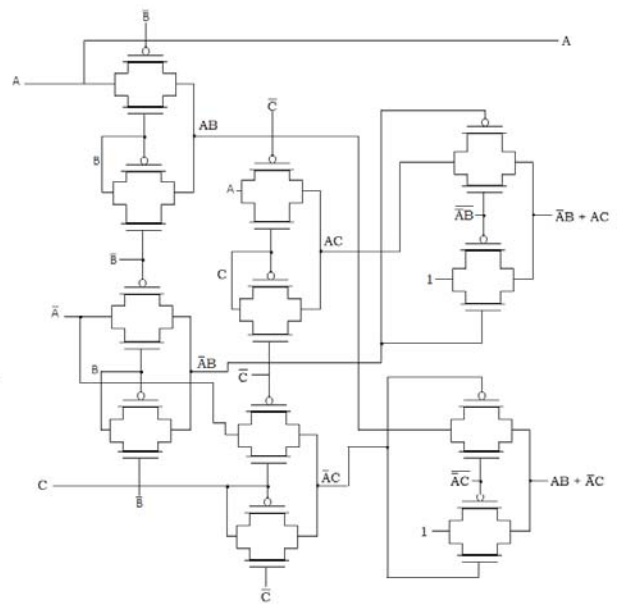
Fig.4. Generalized block diagram for $m:2^m$ Reversible Decoder

C. Transmission Gate based implementation of Feynman and Fredkin gates

A transmission gate (TG) is parallel connection of NMOS and PMOS switch and is shown in figure 5. The inputs X and S (applied to gate terminals) are called pass and control input and the gate provides. The output of TG is represented as Y . When the control signal $S=0$, the output will be in high impedance state while following the pass input (X) for $S=1$. The advantage of TG gate over NMPS or PMOS pass gate lies in the fact that the output is not degraded in the former one. The TG based implementation of Feynman and Fredkin gates is given in Fig. 5.



(a)



(b)

Fig. 5. TG based implementation of (a) Feynman and (d) Fredkin Gates

III. SIMULATION RESULT AND ANALYSIS

The theoretical proposition is verified using SPICE simulations using 0.18 μ m TSMC CMOS technology parameters. Proposed 2:4 and 3:8 reversible decoders have been implemented using the TG representation of FG and FRG gates given in Fig. 5. The aspect ratios of all NMOS and PMOS transistors are taken as 0.2 μ m/0.27 μ m and 0.5 μ m/0.27 μ m respectively. Figures 6 and 7 depict the simulated result for active high mode of operation of proposed 2:4 and 3:8 decoders. Similar results are obtained for active low mode of operation. The simulated results for 2-to-4 and 3-to-8 reversible decoders adhere to their functionality.

The proposed 2:4 and 3:8 decoders are compared with their existing counterparts and are summarized in Table 4. The proposed 2:4 decoder show 50% reduction in the number of constant inputs and garbage outputs as compared to the one proposed in [7] with no increase in quantum cost. Though the proposed 3:8 decoder has a higher quantum cost (12.5%) than [7] but uses lesser number of constant inputs and garbage outputs and an advantage of providing active high and active low mode of operation. Similarly, while comparing the proposed 2:4 decoder with the one given in [8], it is observed that there is 66.67% , 50% and 20% improvement in constant inputs, garbage output and quantum cost. Compared to decoders of Ref. [9], the proposed decoder is better in terms of constant inputs and garbage outputs.

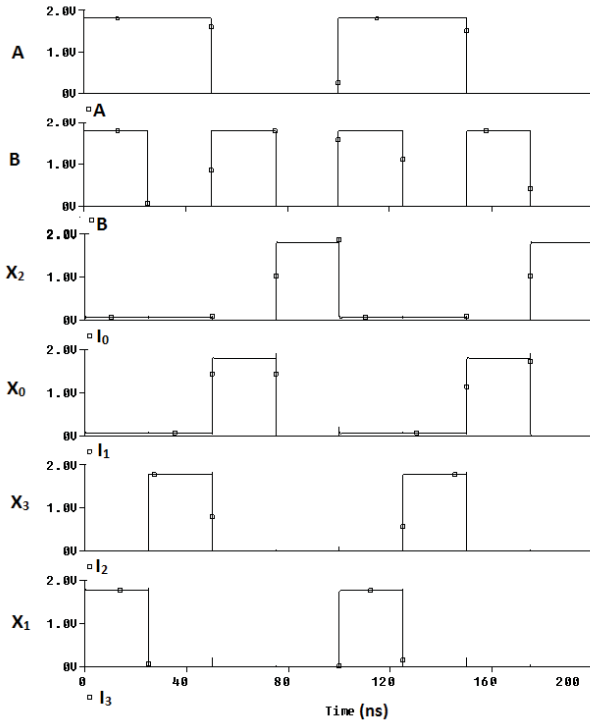


Fig. 6. Simulated waveforms of proposed 2:4 decoder

Table 4 Comparison of Proposed 2:4 and 3:8 reversible decoders with their existing counterparts

Ref. [7]	Constant Inputs	Garbage Outputs	Quantum Cost
2:4 Decoder	4	2	12
Proposed 2:4 Decoder	2	1	12
Percentage Improvement	+50%	+50%	0%
3:8 Decoder	8	3	32
Proposed 3:8 Decoder	6	2	36
Percentage Improvement	+25%	+33%	-12.5%

Ref. [8]	Constant Inputs	Garbage Outputs	Quantum Cost
2:4 Decoder	6	2	15
Proposed 2:4 Decoder	2	1	12
Percentage Improvement	+66.67%	+50%	+20%

Ref. [9]	Constant Inputs	Garbage Outputs	Quantum Cost
2:4 Decoder	3	1	11
Proposed 2:4 Decoder	2	1	12
Percentage Improvement	+33.33%	+0%	-9.09%
3:8 Decoder	8	3	35
Proposed 3:8 Decoder	6	2	36
Percentage Improvement	+25%	+33.33%	-2.85%

IV. CONCLUSION

Reversible decoder of size 2:4 is presented in this paper and the design is extended to 3:8 decoder. The design is generalized to n-to-2ⁿ reversible decoder. The proposed reversible decoders used Feynman and Fredkin gates which are implemented using TG logic. The proposed reversible decoders can be used in active high or active low mode of operation depending upon the select line. The structure is more efficient than its previous counterparts. The cost metrics of the proposed decoder can further be reduced if the select line ‘S’ is assumed not to be the output of any other reversible gate.

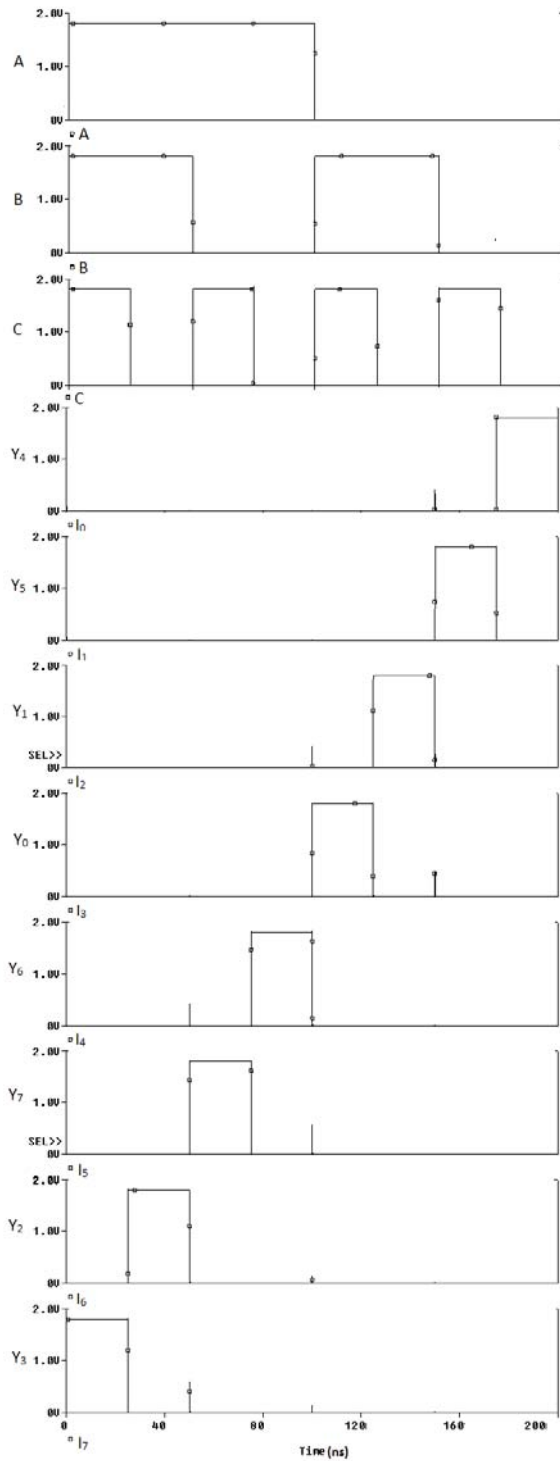


Fig. 7. Simulated waveforms of proposed 2:4 decoder

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