

# Design of Low Logical Cost Conservative Reversible Adders using Novel PCTG

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**Abstract**—Reversible Logic is one of the emerging computing technologies which assures zero power dissipation theoretically through thermodynamically proven principles. Its applications cover a wide spectrum starting with Low Power VLSI, quantum computing, Bio Informatics, Optical Circuits to Nanotechnology based systems. It can take in hand the issues of Fault tolerance through a special class of gates called parity conserving reversible logic gates. This paper aims to study the design a fault tolerant full adders using the new Parity Conserving Toffoli Gate, which is in turn employed to construct ripple carry adders, and high speed adders like carry skip adder. The design has the most optimized performance parameters in terms of Logical Cost than its counterparts in the literature.

**Keywords**— *Reversible Logic Gates, PCTG, Total Logical Cost, Fault Tolerant Full Adder, Quantum Computing.*

## I. INTRODUCTION

It has been shown by Landauer [1] that every bit of information lost will generate  $kT \log_2$  joules of energy  $k$  is Boltzmann's constant and  $T$  is absolute temperature at which computation is performed. Later it was shown by Bennett [2] that this energy dissipation would not occur, if a computation is carried out in a reversible way. Reversible computing is motivated by the Von Neumann Landauer (VNL) principle, a theorem of modern physics which states that ordinary irreversible logic operations which destructively overwrite previous outputs incur a fundamental minimum energy cost. Such operations typically dissipate roughly the logic signal energy, itself irreducible due to thermal noise. This fact threatens to end improvements in practical computer performance within the next few decades. However, computers based mainly on reversible logic operations can reuse a fraction of the signal energy that theoretically can approach arbitrarily near to 100% as the quality of the hardware is improved, reopening the door to arbitrarily high computer performance at a given level of power dissipation.

The primary motivation for reversible computing lies in the fact that it provides the only way (that is, the only way that is logically consistent with the most firmly-established principles of fundamental physics) that performance on most applications within realistic power constraints might still continue increasing indefinitely. The parity conserving reversible logic gates are one class of reversible logic gates that have unique property of fault tolerance derived from

parity conservation techniques which can be efficiently used to design fault tolerant arithmetic circuits.

In this paper we study the new structure for the fault tolerant full adder using the Parity Conserving Toffoli gate, which has been used to design ripple carry adders and carry skip adder. The remainder of the paper is organized as follows: Section II gives the terminologies pertaining to the reversible logic and explains some of the basic as well as parity preserving reversible logic gates. Section III gives the design of the proposed adder whose design is used in ripple carry adder and carry skip adder. Section IV gives the analyses and comparisons of different performance parameters.

## II. REVERSIBLE LOGIC

### A. Terminologies

Some of the basic definitions [10] pertaining to reversible logic are mentioned below. *Reversible Logic Function* is a Boolean Function  $f(x_1, x_2, x_3, \dots, x_N)$  that satisfies the following criteria : (i)The number of inputs is equal to the number of the number of outputs.(ii)Every output vector has an unique pre-image. *Reversible Logic Gate* is an N-input N-output logic device that provides one to one mapping between the input and the output. *Garbage Outputs (GO)* are the additional outputs can be added so as to make the number of inputs and outputs equal whenever necessary. The number of outputs which are not used in the synthesis of a given function are called garbage outputs. *Quantum Cost (QC)* refers to the cost of the circuit in terms of the cost of a primitive gate and is computed knowing the number of primitive reversible logic gates ( $1*1$  or  $2*2$ ) required to realize the circuit.

*Gate levels or Logic Depth* refers to the number of levels in the circuit which are required to realize the given logic functions. *Flexibility* refers to the universality of a reversible logic gate in realizing more functions. *Gate count (GC)* - The number of reversible gates used to realize the function. *Constant Inputs (CI)* refer to the number of inputs that are to be maintained constant (either at 0 or 1) in order to synthesize a given logic function. *Total Logical Cost* – This is measured by counting the number of AND operations, number of EX-OR operations and number of NOT operations. Let  $\alpha$  = No. of EX-OR operations  $\beta$  = No. of AND operations  $\delta$  = No. of NOT operations then the total logical cost  $T$  is given as sum of number of AND, EX-OR and NOT operations.

$$T = N(\alpha) \cdot \alpha + N(\beta) \cdot \beta + N(\delta) \cdot \delta \quad (1)$$

Where  $N(*)$  denotes “number of”

**Total Reversible Logic Implementation Cost (TRLIC):** This parameter [11] is defined as the sum of all the cost metrics of a reversible logic circuit viz., the CI, GC, QC and GO. The TRLIC is a parameter which reflects the overall performance of a reversible logic circuit.

$$TRLIC = \Sigma(CI, GC, QC, GO) \quad (2)$$

### B. Basic Reversible Logic Gates

The basic reversible logic gates that are widely studied in the reversible logic are:

#### 1) Feynman Gate:

It is a  $2 \times 2$  gate with quantum cost of one. It is also called Controlled NOT (CNOT) gate depicting its operation; the gate and its reversible logic circuit [5] are as shown in Fig.1.

#### 2) Peres Gate:

It is a  $3 \times 3$  gate [3] that has input output combination as  $(A \rightarrow P = A, B \rightarrow Q = A \oplus B, C \rightarrow R = AB \oplus C)$ . It is a  $3 \times 3$  gate with a quantum cost of 4.

#### 3) Fredkin Gate:

It is also a  $3 \times 3$  gate [4] which maps inputs  $(A, B, C)$  to output  $(A, A'B+AC, A'C+AB)$ . It has a quantum cost of five and is a parity preserving gate as well as a universal gate.

#### 4) Toffoli Gate:

It is a  $3 \times 3$  gate [4] with input output mapping given by  $(A \rightarrow P = A, B \rightarrow Q = B, C \rightarrow R = AB \oplus C)$ . It has a quantum cost of five and is also a universal gate. Its gate diagram and quantum circuit are as shown in the fig 1.

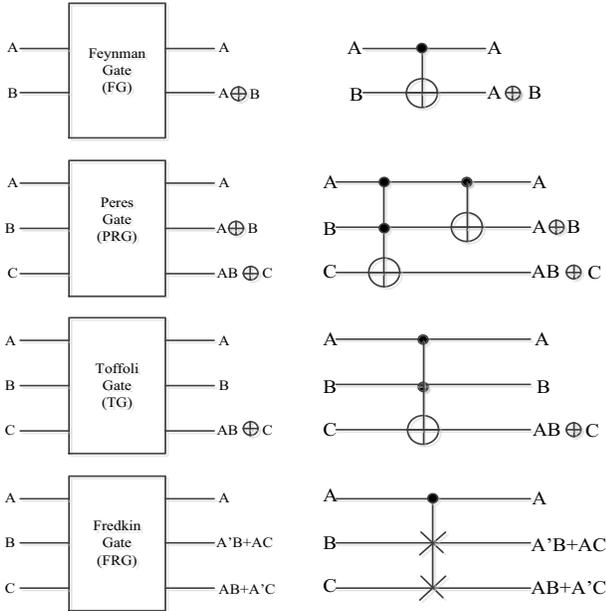


FIGURE 1: BASIC REVERSIBLE LOGIC GATES

### C. Parity preserving Reversible Logic Gates

A reversible logic gate will be parity preserving if the EX-OR of the inputs matches the EX-OR of the outputs i.e., parity of the input and the output remains the same. If  $I_1, I_2, \dots, I_N$  and  $O_1, O_2, \dots, O_N$  are the inputs and outputs of an  $N \times N$  reversible logic gate, it will be parity preserving iff they satisfy  $I_1 \oplus I_2 \dots \oplus I_N = O_1 \oplus O_2 \dots \oplus O_N$ . A sufficient requirement for parity preservation of a reversible circuit is that each gate be parity preserving. Some of the parity preserving reversible logic gates are as follows:

#### 1) Double Feynman Gate:

It is a cascade of two Feynman gates and is the simplest among all. The inputs  $I (A, B, C)$  are mapped to outputs  $O (A, A \oplus B, A \oplus C)$ . It has a quantum cost of two [6]. The gate is as shown in Fig. 2.

#### 2) NFT Gate:

It is a  $3 \times 3$  gate that has input output relation given by  $(A \rightarrow P = A \oplus B, B \rightarrow Q = BC' \oplus AC', C \rightarrow R = BC \oplus AC')$  [12]. It has a quantum cost of five and the gate diagram is as depicted in Fig. 2.

#### 3) Our Proposed Parity Conserving Toffoli Gate (PCTG):

Toffoli is one of the universal gates as well as a self reversible gate i.e. the gate is same as its dual. The dual of a gate is an inverse that reverses its logic function. PCTG [20] is parity preserving version of Toffoli Gate. This gate has a quantum cost of 7 and the reversible implementation is as shown in Fig. 2.

#### 4) Islam Gate (IG), F2PG and PPPG:

It is a  $4 \times 4$  gate [8] that has a quantum cost of 7. F2PG is a  $5 \times 5$  gate whose quantum cost has not been specified by [13]. PPPG is also a  $5 \times 5$  gate [7] and its quantum cost is unspecified. Single F2PG and PPPG gate can be used as a Full Adder.

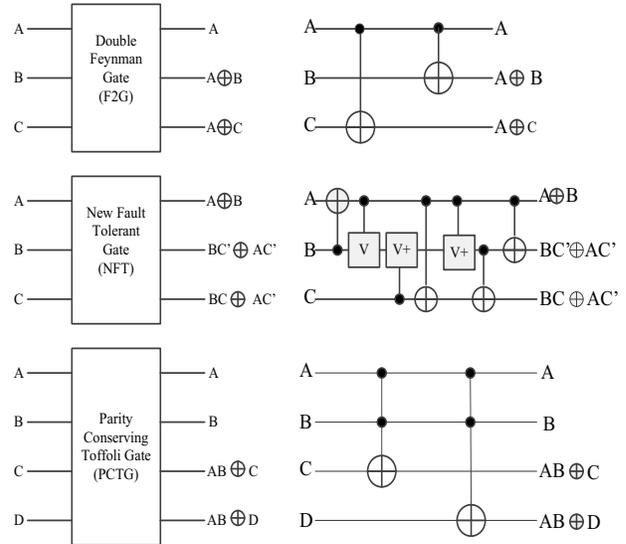


FIGURE 2: PARITY PRESERVING REVERSIBLE LOGIC GATES

### III. PCTG AND PARITY PRESERVING ADDER DESIGNS

Full Adder is one of the most basic and versatile components of most of the arithmetic circuits like the Carry Save adder, Ripple Carry adder, BCD Adder, and even most complex Arithmetic Logic Units. Thus fault tolerant implementation of this full adder structure is basic requisite. There are innumerable attempts in the literature to build full adders using reversible logic gates out of which only handful of them are fault tolerant. Some noteworthy works in this area are enlisted in the next few lines of this section.

A full adder is generally designed using a Toffoli gate. The Toffoli being a non conservative gate, the other parity preserving reversible logic gates are used to design a Parity Preserving Toffoli structure. One such implementation where two Double Feynman and one Fredkin gates are used has been proposed in [17]. The Total Logical Cost of this Toffoli is  $T=6\alpha+4\beta+2\delta$  and the quantum cost is 9. In [12] another such implementation is encountered where the design consists of a NFT and a Double Feynman gate, with Hardware complexity and quantum cost as  $T=5\alpha+3\beta+2\delta$  and 7. [18] has also proposed a fault Tolerant Toffoli gate which uses a Fredkin and a Double Feynman gate with  $T=4\alpha+4\beta+2\delta$  and quantum cost of 7. The proposed Parity Conserving Toffoli Gate (PCTG) can directly be modified to produce Toffoli functionality. These Parity Preserving Toffoli gates are cascaded along with Double Feynman gates in order to obtain a Fault Tolerant Full Adder Structure [16] shown in fig 4.

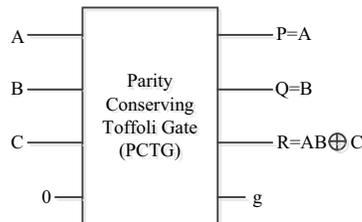


FIGURE 3: PROPOSED PARITY CONSERVING TOFFOLI STRUCTURE

The above four mentioned designs can be substituted in the structure shown in [16] so as to obtain a Fault Tolerant Full Adder (FTFA). [18] has also proposed the IG which can be cascaded to obtain a parity preserving Full adder. [19] has also proposed a Fault Tolerant Full adder which makes use of three Double Feynman gates and one NFT gate. [15] has proposed a FTFA using four Fredkin gates. In [7] and [13] a single gate has been designed that functions as FTFA by setting two of its inputs at constant values i.e., at binary zero.

The ripple carry adder is obtained by series connecting the FTFAs by applying the output carry of one stage to the next subsequent stage. The number of bits that are to be ripple carry added verdicts the number of gates and hence the other performance parameters. The figure 8 shows 4 Bit RCA.

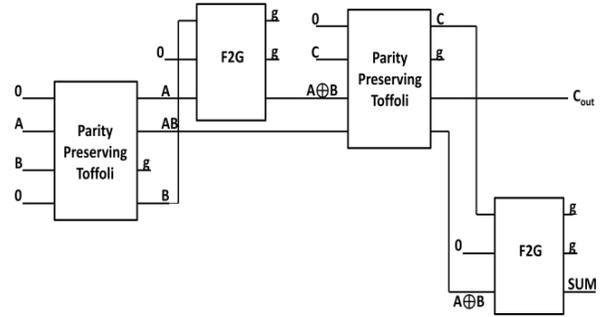


FIGURE 4: FAULT TOLERANT FULL ADDER USING PARITY PRESERVING TOFFOLI [16]

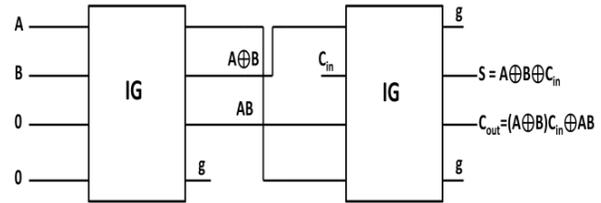


FIGURE 5: FAULT TOLERANT FULL ADDER IN [18]

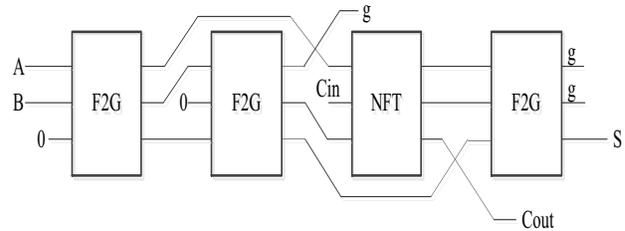


FIGURE 6: FAULT TOLERANT FULL ADDER IN [19]

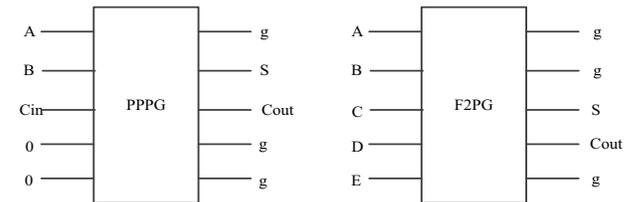


FIGURE 7: FAULT TOLERANT FULL ADDER IN [7] AND [13]

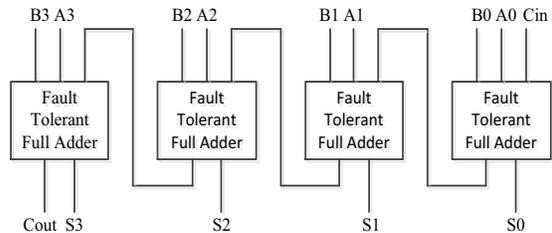


FIGURE 8: FAULT TOLERANT RIPPLE CARRY ADDER



MODELSIM and the simulation results are as shown in figures 10, 11, 12 and 13.

TABLE 2: COMPARISON OF FULL ADDER DESIGNS

Fault Tolerant Full Adder Design	Gates	Total Logical Cost
Proposed Design	2 PCTG+ 2 F2G	$T = 8\alpha + 4\beta$
Design in [14]	2 IG	$T = 8\alpha + 6\beta + 2\delta$
Design in [13]	1 F2PG	$T = 8\alpha + 6\beta + 2\delta$
Design in [15]	4 FRG	$T = 8\alpha + 16\beta + 4\delta$
Design in [19]	1 NFT + 3 F2G	$T = 9\alpha + 4\beta + 3\delta$
Design in [18]	2 FRG + 4 F2G	$T = 12\alpha + 8\beta + 2\delta$
Design in [12]	2 NFT + 4 F2G	$T = 14\alpha + 6\beta + 4\delta$
Design in [17]	2 FRG + 6 F2G	$T = 16\alpha + 8\beta + 4\delta$
Design in [7]	1 PPPG	$T = 11\alpha + 18\beta + 11\delta$

TABLE 3: COMPARISON OF 4 BIT RIPPLE CARRY ADDER DESIGNS

4 Bit Ripple Carry Adder Design	Gates	Total Logical Cost
Proposed Design	8 PCTG+ 8 F2G	$T = 32\alpha + 16\beta$
Design in [14]	8 IG	$T = 32\alpha + 24\beta + 8\delta$
Design in [13]	4 F2PG	$T = 32\alpha + 24\beta + 8\delta$
Design in [15]	16 FRG	$T = 32\alpha + 64\beta + 16\delta$
Design in [19]	4 NFT + 12 F2G	$T = 36\alpha + 16\beta + 12\delta$
Design in [18]	8 FRG + 16 F2G	$T = 48\alpha + 32\beta + 8\delta$
Design in [12]	8 NFT + 16 F2G	$T = 56\alpha + 24\beta + 16\delta$
Design in [17]	8 FRG + 24 F2G	$T = 64\alpha + 32\beta + 16\delta$
Design in [7]	4 PPPG	$T = 44\alpha + 72\beta + 44\delta$

TABLE 4: COMPARISON OF CSA DESIGNS

4 Bit Carry Skip Adder Design	Total Logical Cost	Conservative Nature	Fan-out
Proposed Design	$T = 42\alpha + 24\beta$	Yes	Yes
Design in [21]	$T = 40\alpha + 28\beta + 12\delta$	Yes	No
Design in [15]	$T = 40\alpha + 80\beta + 20\delta$	Yes	Yes
Design in [22]	$T = 32\alpha + 36\beta + 44\delta$	No	No

### CONCLUSIONS

In this paper the different adder structures namely full adder, ripple carry adder have been studied and the Carry skip adder have been designed, starting from the most elementary structure PCTG. This gate is the parity conservative cohort of

the Toffoli gate. It maintains the universality of the Toffoli gate as well as inherits the conservative nature.

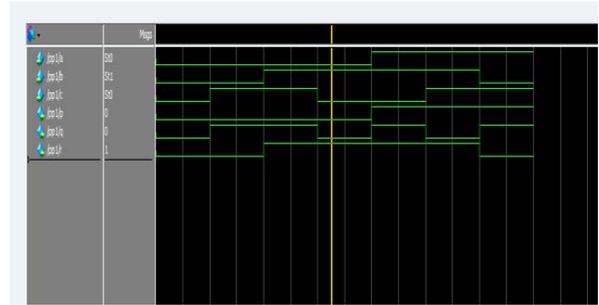


FIGURE 10: SIMULATION RESULTS OF PROPOSED PARITY PRESERVING TOFFOLI STRUCTURE

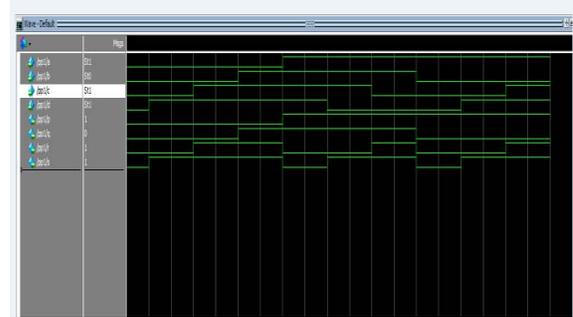


FIGURE 11: SIMULATION RESULTS OF PROPOSED PARITY PRESERVING FULL ADDER

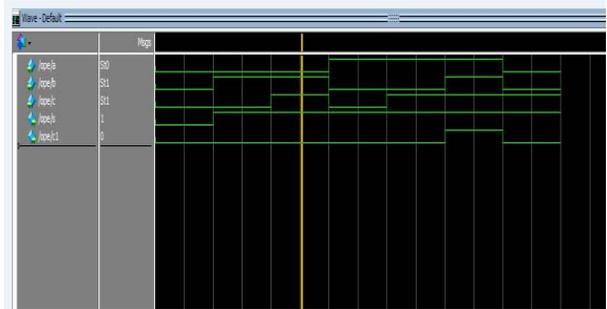


FIGURE 12: SIMULATION RESULTS OF PARITY PRESERVING RIPPLE CARRY ADDER

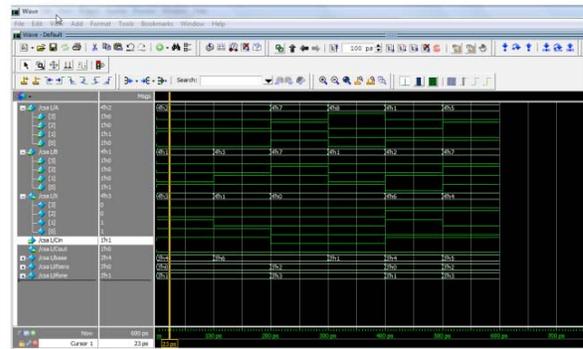


FIGURE 12: SIMULATION RESULTS OF PARITY PRESERVING CARRY SKIP ADDER

The implementation of full adder, which is the most fundamental block of the high speed adders and the ALU, plays a key role in the design aspects of any complex system. In this view the complexity of the full adder itself needs to be minimized so that the complexity of the system reduces. It has been observed that the complexity can be measured using different yardsticks namely the gate count, the quantum cost and the TRLIC. Meanwhile these parameters' scale must be suitably supported by the hardware complexity of the design which is given by the Total Logic Cost. The proposed designs can be said to be the optimized one as they have been derived from the least logical cost PCTG. These structures may be implemented in quantum dot cellular automata, in order to pave a path for further research.

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