Contemplation of Synchronous Gray Code Counter and its Variants using Reversible Logic Gates

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***Abstract*— A Gray Code is an encoding of integers as sequences of bits with the property that the representations of adjacent integers differ in exactly one binary position. Gray Codes have many practical applications that go beyond research interests. There are different types of gray codes: Binary reflected, Maximum Gap, Balanced, Antipodal and Non Composite to name a few. On the other hand Reversible logic has received great attention due to their ability to reduce the power dissipation--an important aspect of low power circuit design. Other applications include Optical information processing, DNA computing, bio informatics, quantum computation and nanotechnology. Counters have a primary function of producing a specified output sequence and are thus sometimes referred to as pattern generators. This paper proposes design of different gray code counters using reversible logic gates, to draw comparative conclusions upon their performance.**

Keywords- Gray Code, Binary Reflected Gray Code, Uniform Balanced Gray Code, Antipodal Gray Code, Reversible logic circuits, Quantum Computation.

I. INTRODUCTION

The power consumption which leads to heat dissipation in computer machinery has become one of the greatest challenge and research interest today. Any computation that can be reversibly performed both logically and thermodynamically, leads to dissipating arbitrarily little energy [1, 2]. R.Landauer in1961 [1] showed that irreversibility in the computing process that leads to loss of information requires minimum heat generation in the order of k*T for each irreversible function, k is Boltzmann's constant and T is the absolute temperature. C.H.Bennett in 1973 [2] showed that an irreversible computer can always be made reversible. Reversible logic circuits naturally take care of heating since in a reversible logic every input vector can be uniquely recovered from its output vectors and therefore no information is lost. According to [2] zero energy dissipation would be possible only if the network consists of reversible gates.

Any reversible gate performs the permutation of its input vector patterns only. If a reversible gate has k inputs, and therefore k outputs, then we call it a k*k reversible gate. Additional outputs added so as to make the number of inputs and outputs equal which are not used in the synthesis of a given function but sometimes mandatory to achieve reversibility are called garbage. The important design constraints for reversible logic circuits are: Reversible logic gates do not allow fan-outs. Reversible logic circuits should have minimum quantum cost. The design can be optimized so as to produce minimum number of garbage outputs. The reversible logic circuits must use minimum number of constant inputs.

The remainder of this paper is organized as follows –Section II gives a quick run through the different reversible logic gates used in this paper. Section III lists the different types of gray codes and the codes itself in a lexicographical order. Section IV shows the design of reversible gray code counter for the different gray codes enlisted in the section III and performs a comparative study.

II. REVERSIBLE LOGIC GATES

The important reversible logic gates and a brief overview of the same are as under.

A. Feynman Gate

It is a 2x2 gate and its logic circuit is as shown in the figure. It is also known as Controlled Not Gate. It has quantum cost one and is generally used for Fan Out purposes.

B. Peres Gate

It is a 3x3 gate and its logic circuit is as shown in the figure. It has quantum cost four.

C. Toffoli Gate

It is a 3X3 gate and its logic circuit is as shown in the figure. It has quantum cost of five.

D. Fredkin Gate

It is also a 3X3 gate. The logic circuit is as shown in the figure. It has a quantum cost of five.

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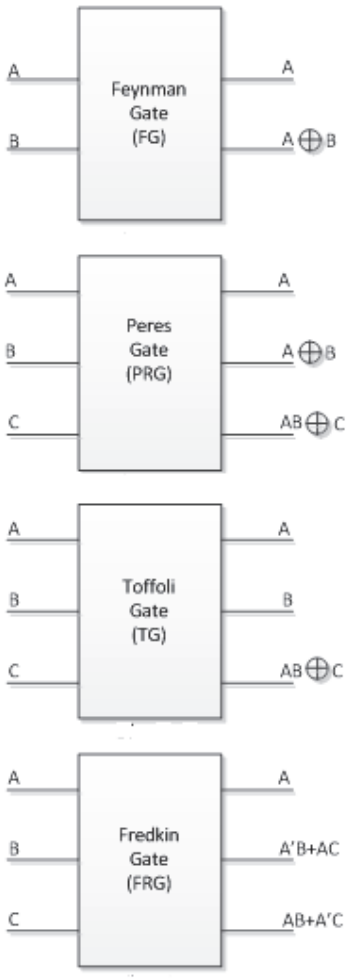

FIGURE 1: REVERSIBLE LOGIC GATES

E. SCL Gate

It is a 4X4 gate. Its logic circuit is as shown in the figure. Its quantum cost is not specified by [8]

F. TR Gate

It is a 3x3 gate and its logic circuit is as shown in the figure. It has quantum cost four.

G. New Gate

It is a 3X3 reversible gate and its logic circuit is as shown. It has a quantum cost of five.

H. URG Gate

It is also a 3X3 gate. Its quantum cost is not specified by [14]. Its logic diagram is as shown in the figure.

I. Sayem Gate

It is a 4X4 gate. Its logic circuit is as shown in the figure. Its quantum cost is not specified by [10].

J. OTG Gate

It is a 4X4 gate. Its logic circuit is as shown in the figure. Its quantum cost is not specified by [9].

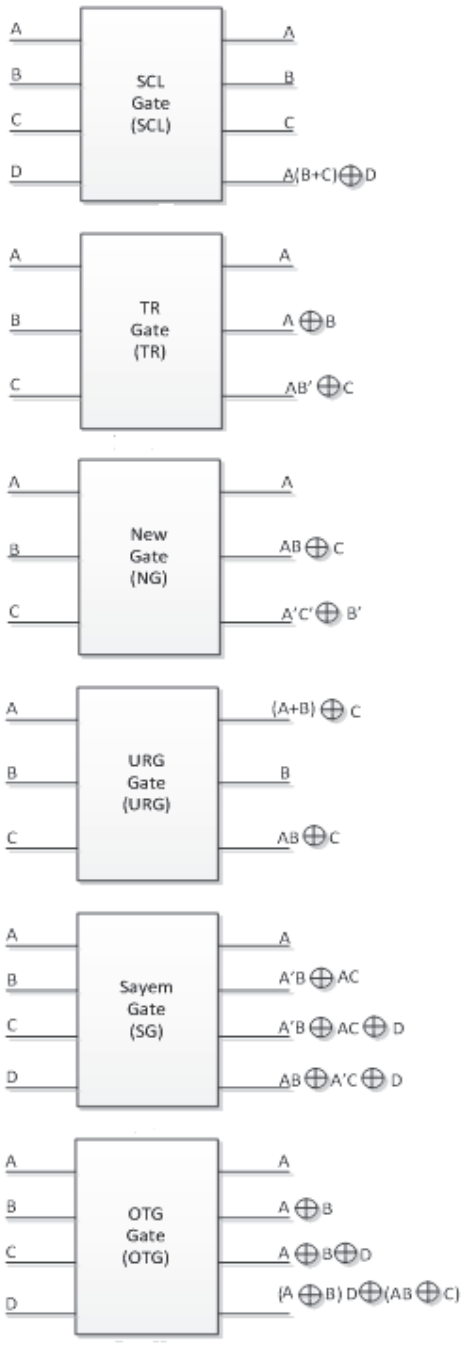

FIGURE 2: REVERSIBLE LOGIC GATES CONTINUED

III. GRAY CODE AND ITS TYPES

A Gray Code is an encoding of integers as sequences of bits with the property that the representations of adjacent integers differ in exactly one binary position. An N-bit Gray Code is a circular list of 2N N-bit binary numbers ordered in such a way that each binary number differs from its neighbor by exactly 1 bit (hamming distance = 1).Some of the widely cited gray codes are given below.

A. Binary Reflected Gray Code (BRGC):

It is the most common form of gray code and vastly superior in communications protocols. The sequence is shown in Table 1 But generally this is not the optimal code for use as output for mechanical actuators where it is preferred to have a coding system that provides more uniformity. Two measures of uniformity are the transition counts and the gap of the code.

B. Uniformly Balanced Gray Code (UBGC):

Gray codes with the additional property that the number of bit changes is more uniformly distributed among the bit positions. The sequence of UBGC in the lexicographical order is tabulated in table 1.

C. Antipodal Gray Codes (APGC):

An n-bit Antipodal Gray Codes have the additional property that the binary complement of any code string appears exactly n steps away in the list. Thus the spatial frequency of the antipodal Gray code-pattern is similar along frames. The code is as shown in Table 1.

D. Maximum Gap Gray Codes (MGGC):

Sometimes it is also required to maximize the gap in a gray code. MGGC are those that have the shortest maximal consecutive sequence of 0's or 1's among all bit positions.

E. Non Composite Gray Code (NCGC):

An n bit NCGC requires that no contiguous subsequence correspond to a path in any k-cube for $2 \leq k \leq n$.

TABLE 1: DIFFERENT TYPES OF GRAY CODES

Binary Reflected Gray Codes		Antipodal Gray Codes		Uniformly Balanced Gray Codes	
0000	1100	0000	1010	0000	0110
0001	1101	0001	1011	1000	0100
0011	1111	0011	1001	1100	0101
0010	1110	0111	1101	1101	0111
0110	1010	1111	0101	1111	0011
0111	1011	1110	0100	1110	1011
0101	1001	1100	0110	1010	1001
0100	1000	1000	0010	0010	0001

In this paper we design reversible gray code counters for binary reflected, uniformly balanced and antipodal gray codes which are the most frequently used ones in the design and technology. (*Note: The unnamed outputs which are not connected to any other gates in Fig. 3, 4 and 5 are the garbage outputs 'g'*)

IV. DESIGN OF GRAY CODE COUNTERS

The general procedure adopted for the design of synchronous gray code counters is as stated. Synchronous counter is characterized by the count pulses being applied directly to the control inputs, C, of the clocked flip-flops that comprise the counter. As a result all the flip-flops change simultaneously and the new state of the counter is observable. The 4 bit counters are designed using clocked D flip-flops. To describe the logic network the present and next state table is written. The inputs to the four D flip-flops are logically deduced from the excitation table of D flip-flop. To complete the design, the present state table is used as input vector and input to the flip-flop is treated as the Boolean function, and minimal excitation expressions for the flip flop inputs can be obtained and implemented using reversible logic gates. A single Sayem gate can realize a D-Latch and in turn a D flip- flop – the constructing element of any sequential circuit.

A. Binary Reflected Gray Code Counter:

The counting sequence is same as that tabulated in Table 1. The reversible logic implementation is as shown in Figure 3.

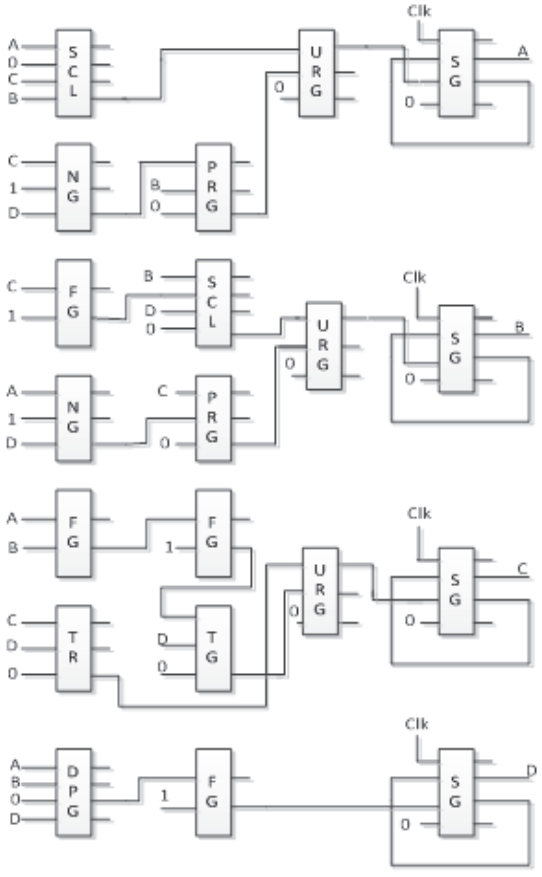

FIGURE 3: BINARY REFLECTED GRAY CODE COUNTER

B. Antipodal Gray Code Counter

The counting sequence is same as that tabulated in Table1. The reversible logic implementation is as shown in the Figure 4.

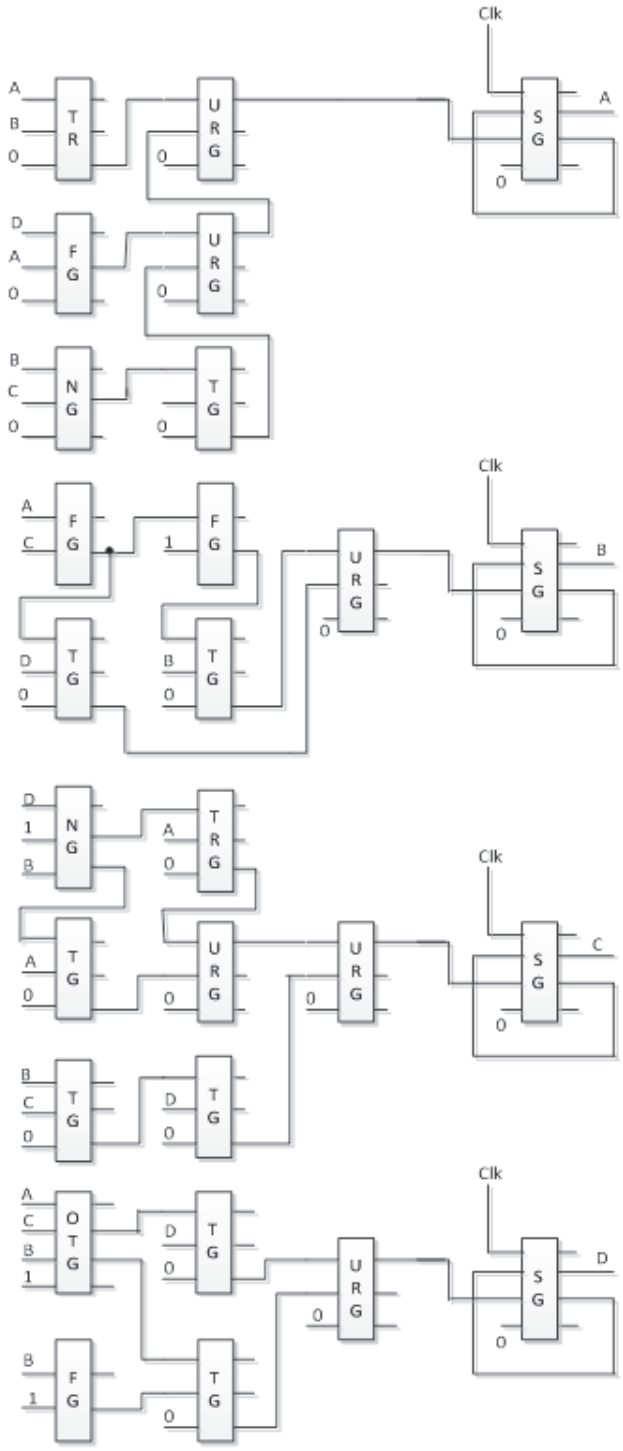

FIGURE 4: ANTIPODAL GRAY CODE COUNTER

C. Uniformly Balanced Gray Code Counter

The counting sequence is same as that tabulated in Table1. The reversible logic implementation is as shown in the Figure 5.

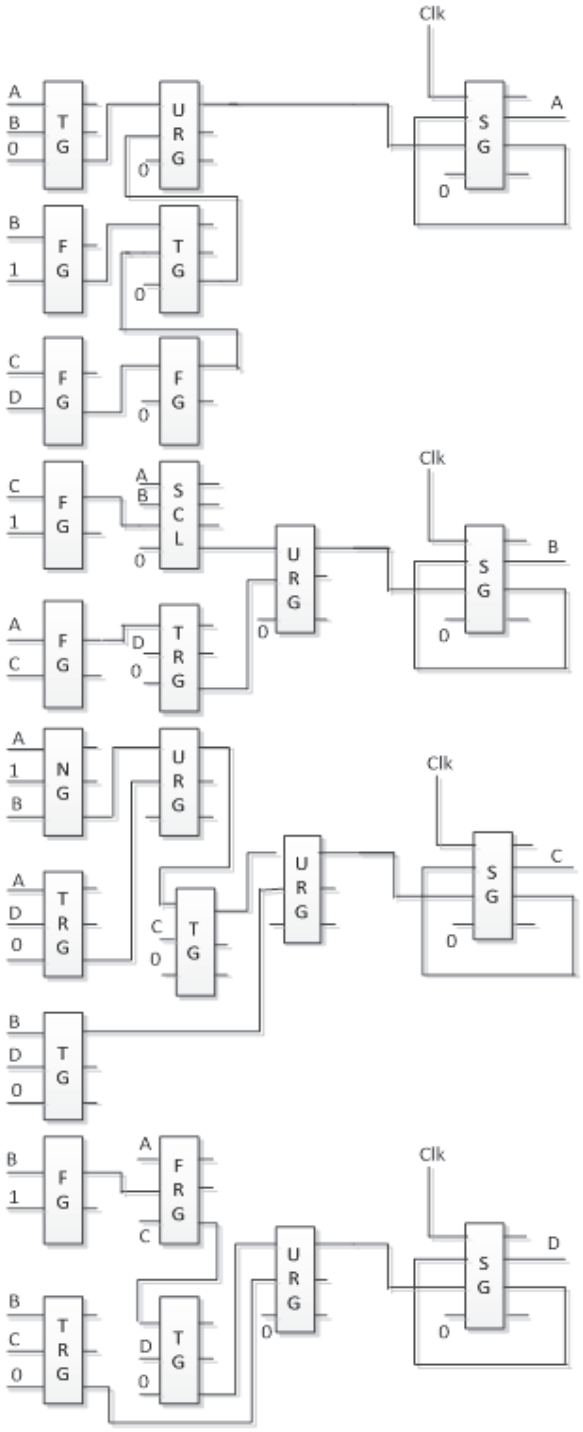

FIGURE 5: UNIFORMLY BALANCED GRAY CODE COUNTER

V. CONCLUSIONS AND SCOPE FOR FUTURE WORK

Gray codes play a major role in research area. Applications span from signal encoding and decoding (Walsh Transforms) digital image processing, data compression techniques, processor allocation in the hyper cube, ordering of documents on shelves, information storage and retrieval, circuit testing, robotics and mechanical encoding to solving puzzles such as Towers of Hanoi and Chinese rings.

Gray Code counters are non glitch counters since only one bit changes. Gray code counters can be used for asynchronous FIFO's address pointers. They reduce the digital noise as compared to the normal counters. They also find application in data path synchronization. They are widely used to facilitate error correction in digital communications such as digital terrestrial television and some cable TV systems.

TABLE 2: COMPARISON OF THE PERFORMANCE METRICS OF THE COUNTERS

Counter Type	No. Of Gates	Garbage Outputs	Constant Inputs	Delay in gate terms
Binary Reflected	20	39	18	4
Antipodal	27	50	26	5
Uniformly Balanced	26	47	22	5

This paper gives a comparative study of gray code variants namely Binary reflected code counter, Antipodal gray code counter and uniform balanced gray code counter. These three variants are analyzed and number of garbage outputs, number of gates and constant inputs associated with each of them is tabulated in table 2. The counters are simulated and verified using XILINX and MODELSIM. The simulation results are shown in Figure 6. The other two variants of gray code counters namely synchronous non composite gray code counter and synchronous maximum gap gray code counter and their implementation using reversible logic circuits are under investigation as future work.

ACKNOWLEDGMENT

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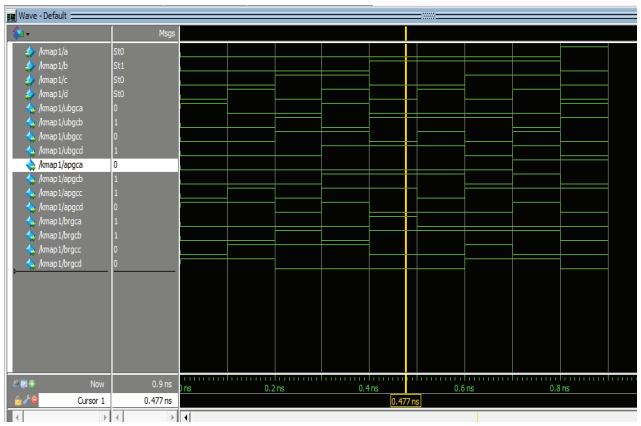

FIGURE 6: SIMULATION RESULTS FOR DIFFERENT GRAY CODE COUNTERS

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